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Electronics

THE MAPLIN MAGAZINE

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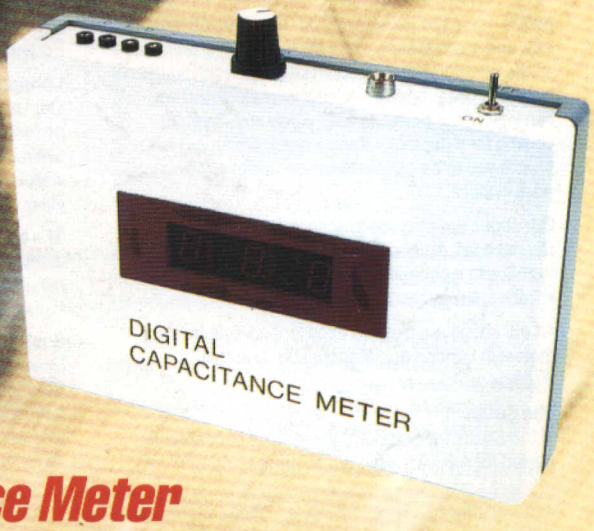
True Stereo TV Sound is coming! Are you switched on to NICAM 728?



Find the value of those unmarked capacitors with our Digital Capacitance Meter

June 1987 to August 1987
Volume 6 Number 23

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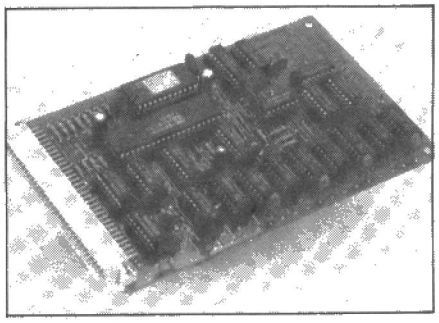
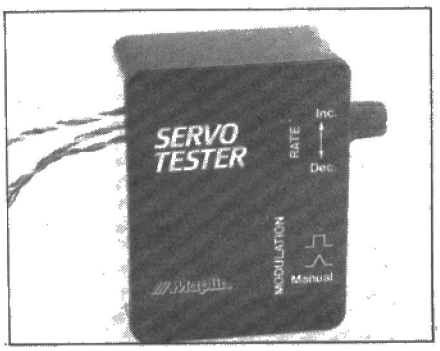
PROJECTS

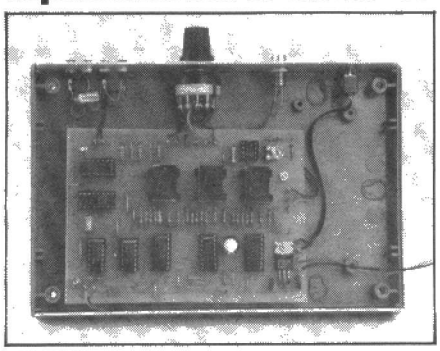


Starting off with a Z80 based microcontroller module using the new Z80-B CPU, capable of running system clock rates up to 6.144MHz. This module has been designed to meet the needs of a wide range of applications, and will be used as part of the Frame Store video display for the WEFAX weather satellite pictures, as part of the MAPSAT series of projects.



Ideal for radio control enthusiasts, this easy to build project can be used to measure the performance of servos and aid fault finding. Proportional servo output is adjustable, with two automatic modes of operation, using the standard format train of positive going pulses in a frame rate of 20ms.

The second part describing the Down Converter for use with the MAPSAT VHF Receiver and Decoder. The installation and testing of the complete system and construction details for the Channel Switching Unit are explained.



Testing capacitors properly is something that is beyond the capability of most multimeters and similar test equipment. Here is a capacitance meter showing values of <9.99nF (100pF minimum) to 99.9μF in five switched ranges on a 3-digit 7-segment LED display.

Another selection of useful circuits which can be easily built on Veroboard, including a Movement Alarm using a mercury switch, a Stepper Motor Driver having an automatic power saving feature, a Pink Noise Generator, Optical Port data link which simply uses your computer's monitor screen, and a 'Metal Pedal' effects unit for producing metallic sounds.

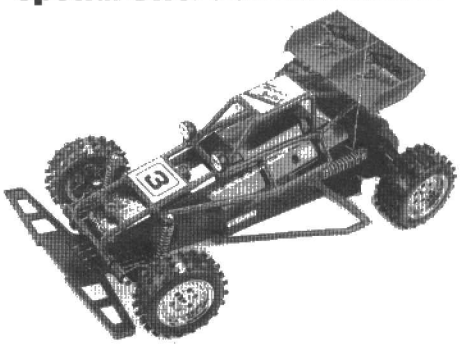
FEATURES

The TV receiver industry is currently in need of something new to boost the sales of sets, as not much has happened since the advent of 625 lines and colour some years ago. Apart from digital video processing (as described in a previous issue) stereo TV sound would seem to be the way to go. Unfortunately, the technical complexity required to achieve this is enormous, since it requires squeezing a phase-encoded stereo sound image into a signal band already fully crowded. Will enough sets sell to make it worth the cost of developing the chips alone?

All about taking measurements with the help of electronic circuitry.

In the last part we saw how important it is to make sure the correct specification transistor is chosen for the task required of it. As far as FET's are concerned, this is probably even more critical as they tend to be specialised, and, between same type devices, they often exhibit electrical tolerance differences wider than may be expected from bipolars.

Part 7. Here we find out how to make the Z80 communicate with the big outside world. The use of peripheral interfacing and I/O ports is explained with programming examples.



The Second World War. A secret weapon was required to stave off the German invasion in 1940, but it was not going to be the "invisible 'Death Ray' which could kill a sheep at one hundred yards." Instead it was discovered that radio emissions could be reflected from aeroplanes in flight, and so RADAR was born.

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NICAM 728

BRITISH DIGITAL STEREO SOUND FOR TELEVISION

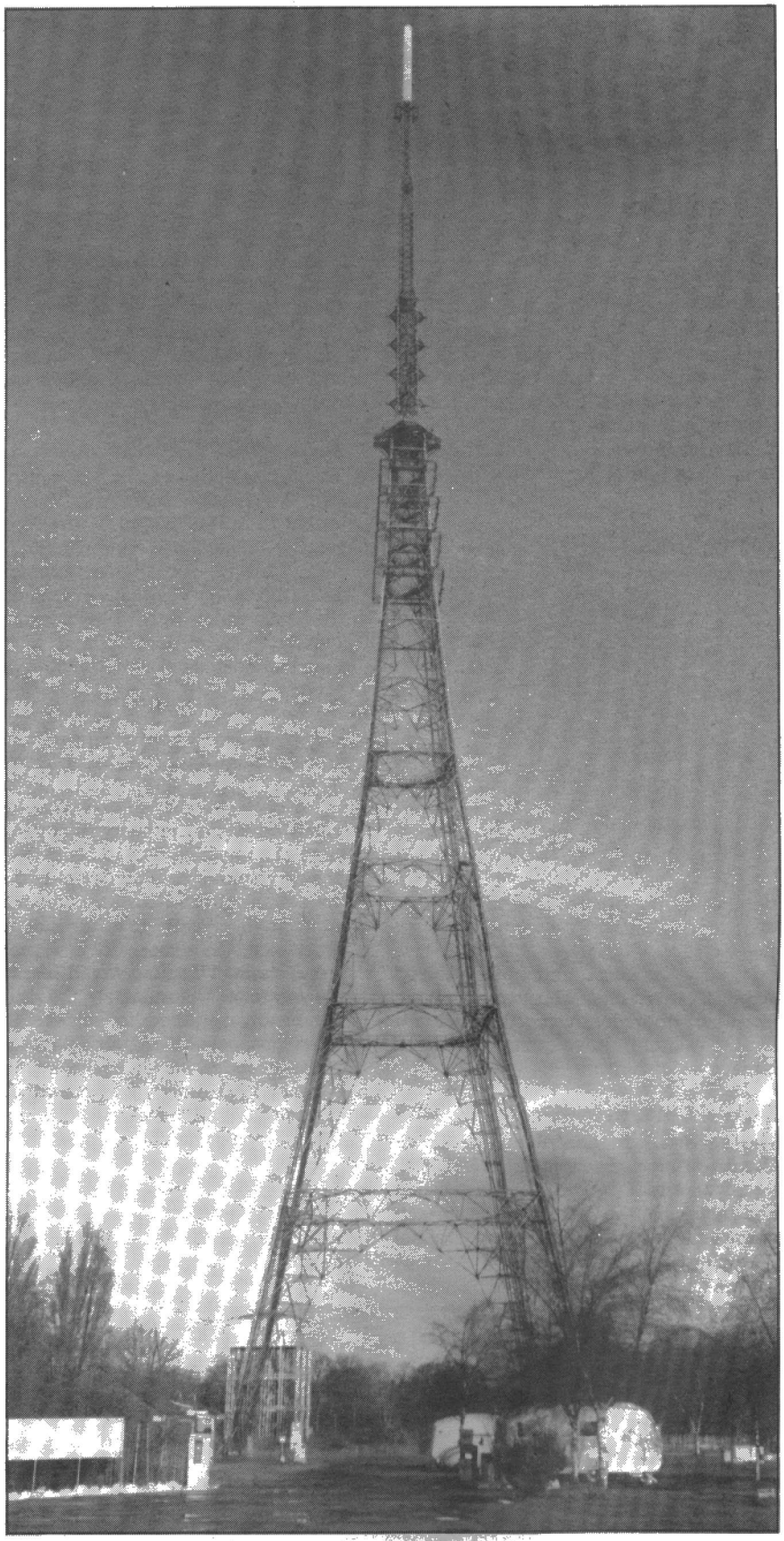
by J.M. Woodgate

B.Sc(Eng.), C.ENG., M.I.E.R.E., M.A.E.S., M.Inst.S.C.E.

By 1990, Britain will have the world's most advanced, high-quality stereo sound system for land-based television. Added to this will be facilities for a number of new data services, either for the public or for closed user-groups. Experimental transmissions are already taking place on the BBC programmes from the Crystal Palace transmitter, and these will be extended in due course. First the Sutton Coldfield and Emley Moor transmitters will be adjusted to accept the stereo signals, followed by a step-by-step conversion of the remaining main transmitters of the UHF network.

New Equipment and Training

Part of the reason for this extended programme of conversion is the need to equip all the studios with stereo audio equipment, including a new system for 'sound-in-syncs' distribution of stereo signals with their associated video, both from within studios and from the studios to the transmitters. It is also necessary for programme producers to learn how to



The Crystal Palace Transmitter.

handle stereo sound in conjunction with the pictures so that viewers are not presented with ridiculously conflicting visual and audible images, such as a distance shot of a band with close-up sound, or a person centre-shot with sound from far right. And not least of the reasons is the need to spread the costs of conversion over a number of years, to avoid too great a burden on the broadcasters' finances, particularly the BBC's.

Transmitting Stereo

We already have a perfectly good method of transmitting stereo sound on FM radio. In particular, it satisfies very well the essential criterion of giving a compatible mono sound signal, which is required by the 20 million mono TV's (and most of the so-called 'stereo' TV's on sale at present!) spread around Britain. Unfortunately, without modification it doesn't work when combined with a television signal, and it has another, inherent limitation that doesn't matter when it is used for sound radio broadcasting in this country.

The first problem is due to 'beating' of the 19kHz pilot-tone and its harmonics, (the vestigial sub-carrier at 38kHz and sub-carriers at 57kHz and 76kHz which may be used for subsidiary services such as 'store-casting' and data transmissions), with the 15.625kHz line-scanning frequency and its harmonics. The slightest non-linearity (distortion) in the transmitter or receiver would cause these beats, and a few moments with the calculator, or a good look at Figure 1, will show that beat-notes would cover the audio band from 1.25kHz upwards. This could be overcome by using the line-scan frequency as the pilot-tone frequency. This is the basis of systems in use in the USA and Japan, where the line frequency is 15.75kHz. However, this means limiting the audio bandwidth to about 12kHz at the most, and the practical systems use a good deal of analogue signal-processing, compression and noise-reduction, to achieve acceptable performance. Buzz on sound due to cross-modulation from the vision signal is still a problem.

Dual-Mono Sound

The second problem with the pilot-tone system is that the maximum realisable separation between channels, measured over the whole transmission-reception chain, is in the region of 40dB. This is more than adequate for stereo, (a reduction of separation from infinity to 40dB moves an extreme left or right image by less than an inch in a typical listening-room arrangement), but is not sufficient to allow the two channels to be used for different signals, such as two different language sound-tracks for a film. For this, at least 60dB separation is necessary, and there is a definite requirement for this feature from the television programme planners. Perhaps the radio planners will also ask for it (or have already?), but there seems no way of providing it for them until Band II is replanned, perhaps next century.

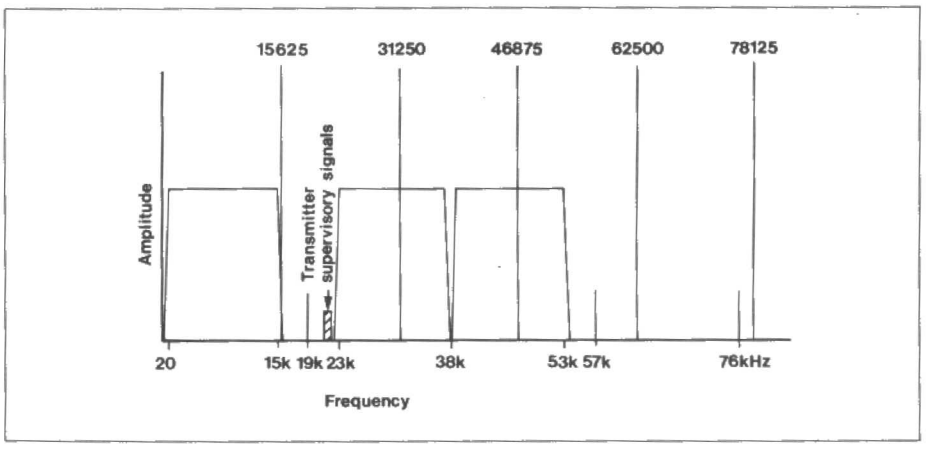


Figure 1. Spectrum of 19kHz pilot-tone stereo signal with 15.625kHz line-frequency harmonics.

The German System

One way of achieving more separation than the pilot-tone system can offer is to use two sound carriers instead of one. For the 625-line television transmission systems B and G (which are only slightly different) used in Germany and several other Continental countries, the sound carrier frequency is 5.5MHz above the vision carrier frequency, and the channel bandwidth is 7MHz (8MHz for system G). There is just room for another sound carrier at 5.7421875MHz, the difference between the carrier frequencies being 15.5 times the line frequency. A system like this is operated in Germany on the second-programme chain, but only a few stereo programmes are broadcast each week. In Britain, system I is used, with the sound carrier 6.0MHz above the vision carrier, and 8MHz channels. There is room for a second sound carrier at about 6.3MHz, and the BBC have tested such a system, but the high level of the additional narrow-band signal makes much more difficult the avoidance of video cross-modulation in the transmitter or receiver, leading to buzz interference on the sound or patterning on the picture, or both. This is particularly difficult to avoid when long chains of relay transmitters are used, as is the case in South Wales.

British Research

The BBC began to look at possible stereo systems for television in the early 1970's, and a considerable amount of testing was carried out on the Japanese and German systems described above. The US system has only recently been defined, but earlier US proposals were also evaluated. At the same time, the possibilities of a digital system were investigated, and the results of other work, on digital systems such as teletext, and satellite broadcasting, were noted for the research on stereo transmission. It was known from theory, and proved in the field with teletext, that digital systems are more sensitive than analogue systems to the effects of multi-path propagation ('ghosting' in television). This is because receiving a digital signal requires the very reliable detection of the presence or absence of a pulse, and if a '0' (no pulse) time interval is partly filled by a delayed '1' signal (the ghost), as shown in Figure 2, detection of the '0' will be difficult or even impossible. On the other hand, a digital system could give better sound quality, less noise, no buzz problems and more than adequate separation for two different language channels. By the early 1980's, a practical digital system had been described by engineers from BBC Research Department, and, after consultation with the IBA and the British receiver manufacturers, final Government approval was given to the system, known unofficially as 'NICAM 728', in September 1986.

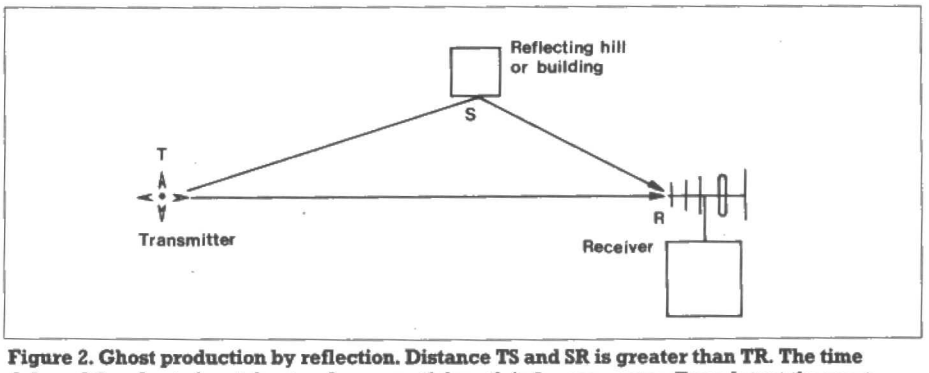


Figure 2. Ghost production by reflection. Distance TS and SR is greater than TR. The time delay of the ghost signal due to a longer path length is 3ns per metre. For teletext the most critical time delay is 288ns, corresponding to a path difference of only 96m and a ghost displacement of 2.2mm on a 53V (22 inch) tube. This is only visible as a lack of horizontal definition. For NICAM 728 the critical delay is 2.74μs, the corresponding path difference is 914m, and the ghost displacement is 2.2cm, clearly visible as a second picture.

Providing Receivers

During the later period of research, the British receiver manufacturers were brought into the picture, and the problems of receiver design and supply were addressed. The major consideration involved the development of the necessary IC's for the receiver. The digital signal goes through an enormous amount of processing at the transmitter, as we shall see, and all this has to be 'unravelled' at the receiver. It would be incredibly expensive to do this without LSI chips, and these just aren't worth designing, at household product prices, unless there is a market in the million size bracket. This in turn means that it is a very important development if some other countries decide to adopt the system, thereby increasing the size of the market for chips. Luckily, considerable interest *has* been expressed by Denmark, Finland, Norway and Sweden, together with other countries outside Europe, such as Hong Kong, and chip development in Britain is now at a reasonably advanced stage. The European Broadcasting Union (EBU) is likely to adopt the British system as the preferred system for digital stereo sound for terrestrial television broadcasting.

Generating the Digital Signal

From all the technical articles and arguments about Compact Disc, it is generally well-known that for the highest quality audio reproduction in the home, 16-bit digital encoding of the analogue signal is required. This gives a signal-to-quantisation noise ratio of about 96dB, and means that in any likely household hi-fi system the dynamic range will be limited by the ambient acoustic noise (flies stamping their feet, pins dropping, etc.), rather than by the quantisation noise reproduced from the loudspeakers. It also means that it is a tough job designing the (analogue) pre-amp and power amplifiers so that they do not degrade that 96dB ratio too much.

Sixteen bit coding is, however, too much of a good thing for broadcasting. It is too wasteful of radio spectrum space, and in any case the ultimate 96dB signal-to-noise ratio cannot be obtained without very expensive receivers and/or a very restricted transmitter service area. The BBC has for a long time been sending stereo sound broadcasting signals around the country on microwave links, using a special form of 14-bit coding, called 14/10 NICAM, in which only 10 bits are actually used for the audio signal. This uses a digital form of the principle of compression/expansion noise-reduction used by proprietary analogue noise reduction systems.

NICAM

NICAM means 'Near-Instantaneous Companded Audio Multiplex'. Companding means COMPression at the transmitter and exPANDING at the receiver. What happens is that the audio signal is first of all encoded in 14-bits, and the resulting 14-bit digital words are divided into blocks of 32. These are then processed digitally, word-by-word, according to the following rules, leading to the coding scheme shown in Figure 3.

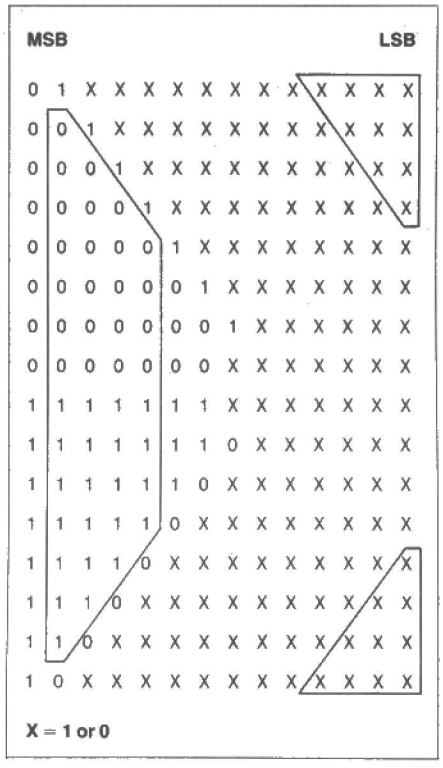


Figure 3. Compressor coding scheme. Bits in the outlined boxes are not transmitted.

Coding Rules

1. The most significant bit (the 14th bit) is passed unchanged.
2. The 13th bit is dropped if it is the same as the 14th.
3. The 12th bit is dropped if it is the same as both the 13th and 14th.
4. The 11th bit is dropped if it is the same as the 12th, 13th and 14th.
5. The 10th bit is dropped if it is the same as the 11th, 12th, 13th and 14th.
6. If the above processes result in a word length longer than 10 bits, enough bits are dropped at the least-significant end to reduce the word length to 10 bits.

Then 'scale' bits are added, together with the parity, synchronising and error-correction bits that have to be squeezed into a practical digital signal. These 'scale' bits tell the expander in the receiver how big the largest sample in each block should really be. This information only has to be sent at a rate fast enough to allow the reconstruction of the fastest audible loudness transition, instead of at the sampling rate, which is what the unprocessed digital signal does. In other words, all the 32 words in a block are assigned the same scalefactor, although this will sometimes not be optimum. Wrongly scaled words are associated with increased quantisation noise in the recovered analogue signal.

Actually, the scale factor information is sent by modifying the parity bits according to a complicated rule which very nearly results in getting something (the transmission of scale factor data) for nothing (no extra bits needed). This can be done because the scale factors are transmitted 32 times in each block, and it is even possible to include additional 'protection range' information which allows receivers to correct errors in the most significant bits of each sample. These scale and protection data can be extracted from the parity bit-stream in the receiver by using majority-decision logic.

In the receiver, the recovered signal has only 10-bit resolution, giving a signal-to-noise ratio of 60dB, but the reference level for the 60dB (i.e. the signal voltage corresponding to 0dB) tracks the peak level of the signal in 1ms intervals. Because the louder signals 'mask', and thus render inaudible, the higher level of noise that comes with them, the effective signal-to-quantisation noise ratio is nearer 84dB, as in a full 14-bit system.

Why NICAM 728?

For the practical system developed by the BBC, the maximum audio frequency that the system will pass was set at 15kHz, as for f.m. radio. The difference in subjective quality between a 15kHz bandwidth and the full 20kHz audio bandwidth is very small. The digital sampling frequency has to be at least twice the audio frequency, with some allowance to ease the design of anti-alias and reconstruction filters, and 32kHz was chosen. Thus the 32-word blocks in the compression process have a time duration of 1ms, and this is consequently the maximum duration of non optimum scaling due to the companding. Such effects appear to be subjectively acceptable, even imperceptible. It is very unlikely that a succession of blocks would all contain large amounts of non-optimum scaling, because the scale-factor is re-calculated for the largest sample in each block.

To carry two digital audio channels of 10-bit words with a sampling rate of 32kHz, we need a bit rate of 2 x 10 x 32 = 640k bit/s as an absolute minimum. However, at least one parity bit is required per word, and it is helpful for decoder design if the sampling frequency can be recovered from the bit clock by division, so a bit rate of 2 x 11 x 32 = 704k bit/s is convenient. However, if the digital audio is slightly time-compressed, to allow a further 24k bit/s for synchronisation or 'framing', control bits and some additional data, the signal format can be the same as that adopted for the C-MAC/packet system of sound and data transmission developed for DBS (Direct Broadcasting by Satellite). This sets the data rate at 728k bit/s, and explains, finally, the system name, NICAM 728.

Snags

You might think that the signal had already undergone more than enough processing, but there are remaining

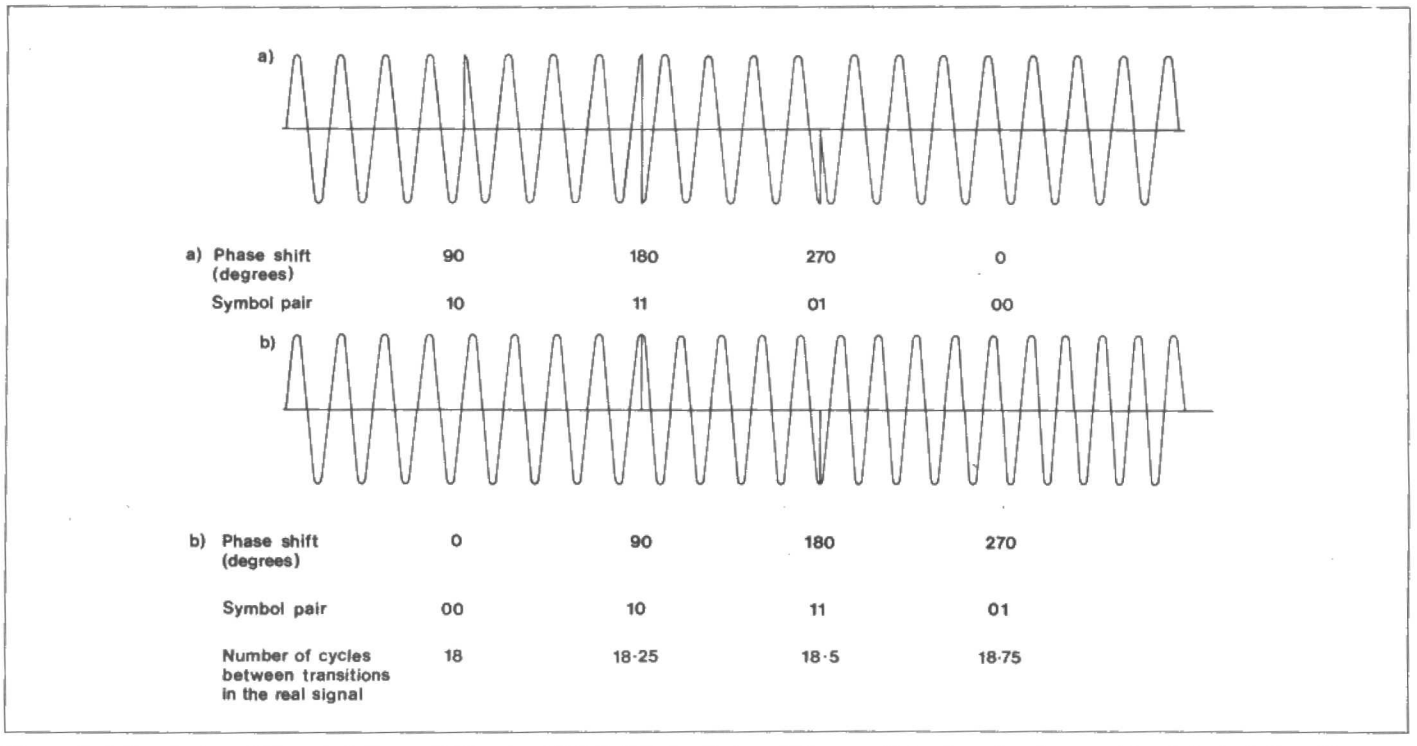


Figure 4 (a). Quadrature differential phase-shift keying (QPSK). This is what would happen if the data signal was not band-limited. Actually, there should be 18 cycles of carrier between the transitions, but the diagram would be too large for the magazine. (b). Quadrature differential phase-shift keying (QPSK). Approximate representation of the effect of band-limiting the data signal. The phase change occurs progressively during the 18+ cycles of carrier (represented as 4 cycles in the diagram). The 'glitches' at 90 and 180 degrees are due to the plotter program, but help to mark the transitions.

problems to be overcome. First of all, if the digital signal were transmitted bit-by-bit in order, multiple-bit errors would certainly cause disturbing noises, and might cause the receiver to lose sync or falsely synchronise, leading to the reproduction of bursts of garbage, much longer than the original error. This is overcome by re-arranging the order of, or 'interleaving', the bits, so that multiple-bit errors affect one or two bits in many words, instead of all the bits in a few. But there is still more to be done.

As it stands, the digital signal has strong harmonics, especially at multiples of 728kHz, which would cause interference with the video signal and possibly with signals on the adjacent channel. There is only spectrum space for a signal of 700kHz total bandwidth, whereas, for example, normal amplitude modulation would require a bandwidth of at least 1456kHz. Clearly, something a little more clever is required. The solution depends on two steps – using a modulation system that is very economical in bandwidth, without being very expensive to demodulate in the receiver, and spreading the spectral energy of the modulated signal by adding a 'random' component. This allows the higher sidebands to be filtered off without losing too much of the wanted information, and also reduces considerably the visibility or audibility of any interference from the digital signal to the vision or mono sound signals. In practice, it is not possible to use a truly random 'energy dispersal' signal, because there is no way of subtracting it in the receiver. But it is possible to generate digital signals which have most of the properties of random signals, yet are totally predictable. These are called 'pseudo-random binary sequences', and all you need to make one is a clock oscillator and a shift register with taps at the right stages, feeding back to the input. These are cheap enough for use in receivers.

The Modulation System

Phase-modulation itself is not well known, so we had better start at the beginning. We can convey information on an r.f. carrier by the familiar methods of either varying its amplitude (a.m.) or frequency (f.m.). We can also do it by changing the *phase* of the signal, and if the modulating signal is digital, these changes will occur abruptly, and between them the carrier signal will be sinusoidal, as shown in Figure 4a. However, it turns out that we can filter out all the sideband's energy except that within half the symbol rate of the carrier frequency (thus 'smearing out' in time the abrupt phase-change), and still detect that it has occurred, i.e. detect the modulation. Once detected in any form, we can easily regenerate the original rectangular digital waveform. If the modulation process is linear, we can obtain the same effect as with filtering the sidebands with a band-pass filter by filtering the modulation signal with a low-pass filter. Such a filter converts a rectangular wave-train (e.g. a data signal) into a triangular wave-train. This effect can be seen in Figure 4b, where the carrier is shown with linear triangular-wave phase-modulation. This is not quite what happens in the real equipment, because the real filter response has not been used. In practice, it is not possible to make the ideal filter, so a larger bandwidth (700kHz instead of 364kHz) has to be accepted.

There are quite a number of different ways of phase-modulating a carrier with a digital signal, and they all have their own strong and weak points. The system chosen for stereo television is called – wait for it – 'Differential Quadrature Phase-Shift Keying', or DQPSK. No-one seems to find anything odd about that word 'keying', which really is a survival from Morse code.

DQPSK

We can explain what happens in two stages. First, we divide up the bit-stream into pairs of bits. Then we shift the phase of the carrier at the start of each two-bit period by a multiple of 90°, according to the following plan:

Input bits	Phase shift (degrees)
0 0	0
1 0	90
1 1	180
0 1	270

Since the phase changes occur after every two bits, and are ¼-cycle changes, we have moved the important first-order sidebands in from 728kHz to 182kHz by using this form of modulation. It is not possible to go on indefinitely saving bandwidth in this way, by grouping the bits into, say, blocks of four, with 45° phase changes, because these smaller changes are more difficult to detect, even digitally.

The carrier frequency has to be above the mono sound carrier at 6MHz, and there are advantages in making it a multiple of the bit-rate. Nine times

728kHz is 6.552MHz, and this frequency has proved satisfactory for System I. It is not so easy to choose the carrier frequency for System B, because 8 x 728kHz = 5.824MHz. This is too close to the mono sound carrier at 5.5MHz to fit in the digital signal, which has a half-bandwidth of 364kHz, but 5.85MHz is usable if the sideband filter is modified.

The bit-pairs could be made up of any two bits, but in fact they are chosen to be corresponding bits from the left and right channels. When two different languages are being broadcast, the two language signals are sent in alternate frames.

Sound Carrier Levels

It is usual for the (mono) sound carrier to be transmitted at a lower power than the peak vision carrier power. This gives the same service area for vision and sound (or rather better for the sound, in many cases), while economising on transmitter power. The exact relative power level is also affected by the need to minimise intermodulation. In this country, improvements in receivers have led to the intention, quite apart from the introduction of stereo, to reduce the relative level of the mono sound carrier from −7dB relative to peak vision carrier to −10dB. With this level of mono sound carrier, the digital carrier level can be set at −20dB with satisfactory results. Interference between the sound signals, and interference from and to the upper adjacent channel vision signal (whose vestigial sideband spectrum overlaps the digital sound signal!) are predicted, on the basis of laboratory and field trials, to be imperceptible, or at worst not disturbing, within the existing transmitter service areas, and in many cases well outside them. It has also been verified that the digital signal will not significantly worsen the effect of co-channel interference to or from the French television transmissions using System L/SECAM, which have an a.m. sound carrier at 6.5MHz. The system will also work for cable television, with some slight processing, easily done at the cable head end.

Complete Digital Signal

We can now put all the parts of the digital signal toegther, and the result is shown in Figure 5.

Frame Alignment Word

This is the digital equivalent of a synch pulse, and is always sent as the 8-bit word 01001110. The energy-dispersal signal is, naturally, not added to these bits. The receiver PRBS generator is synchronised by resetting it on the last bit of this word.

Control Bits

These are five bits which tell the receiver what kind of information is being sent:

C0 is set to 1 for eight frames, and then to 0 for eight frames. This acts as synch information for the decoding of the remaining 4 bits, which may only be altered at frame rate.

C1, C2 and C3 form a 3-bit word, with the following meanings:

000 Stereo signal; alternate left and right channel samples.

010 Two different mono signals, transmitted in alternate frames.

100 One mono signal and one data signal in alternate frames.

110 One data signal at 704k bit/s. No sound.

Note that one bit hasn't been set to 1 in the above words. Setting it allows four more options which are not defined yet.

C4 is set to 1 if the f.m. modulation of the main sound carrier is carrying the same sound programme as the digital signal (or as one of the two mono signals), and to 0 otherwise.

Receivers can thus be designed to switch to f.m. sound if the digital signal fails, and to reject data signals or restricted-access digital sound transmissions.

Additional Data Block

Eleven bits are available for future applications, about which the broadcasters are saying nothing at present. Three eleven-bit words are enough to give over 8.5 billion TV's a unique address code each, so your TV *could* be disabled in less than 3 seconds if you haven't paid the licence fee! (Not that there is any suggestion to introduce such a scheme.) It would also be *possible* to stop off-air video recording, but for land-based transmissions that isn't likely to be politically acceptable now (unless the record manufacturers create a precedent by winning the battle to prevent digital audio tape recorders actually recording anything).

Sound or Data Block

704 bits, either all sound or all data. We have dealt with the structure of this block as far as sound is concerned, and the format(s) for data is not decided yet.

f1 f2 f3 f4 f5 f6 f7 f8 c0 c1 c2 c3 c4 a0 a1 a2 a3 a4 a5 a6 a7 a8 a9 a10 ..... 704 sound or data bits

Figure 5. Complete digital signal.

The UHF Transmitter

Some changes are necessary in the UHF transmitter in order to add in the digital signal on its 6.552MHz carrier, and to ensure an acceptably low level of intermodulation between the output signals.

The digital carrier is first frequency-changed to the appropriate UHF, which is added into the transmitter at a power level of about 0dB(W). The sound and vision signals are amplified by separate klystron UHF tubes, and the sound klystrons have to be tuned to a broader bandwidth to pass both the new and old sound signals. Furthermore, for the f.m. mono sound signal alone the klystrons can be operated in a saturated (non-linear) mode (similar to Class-C with conventional tubes). Were the second carrier to be just added in, there would be a large amount of intermodulation due to the non-linearity. So the operating points of the klystrons have to be set for more linear operation, and the f.m. sound carrier level reduced by 3dB. A certain amount of cancellation of intermodulation products is possible with some transmitter designs, and the end-result is a satisfactory performance with the new signal format.

This completes the description of the digital signal and its transmission, and we now go on to look at the receiver requirements.

Basic Television Receiver

A block diagram of the sound section of a modern TV receiver is shown in Figure 6. This employs what is known as 'quasi-parallel' sound reception, where the sound i.f. carrier is extracted after the first i.f. amplifier; thus it shares the tuner and first i.f. circuits with the vision signal. Older receivers used 'intercarrier' reception, where the sound sub-carrier is filtered off at the video detector: this gives less problem with tuner drift (corrected by digitally-controlled a.f.c. in modern tuners) but more video intermodulation. It may still be possible to use it in digital-stereo receivers, but the buzz level will compromise the signal-to-noise ratio.

Adding the Digital Decoder

Although it is not practicable to modify many existing receivers, even those with stereo audio stages, the addition of the digital sound channel to new designs is fairly simple. As shown in Figure 7, access to the first i.f. stage output is required, from which the digital

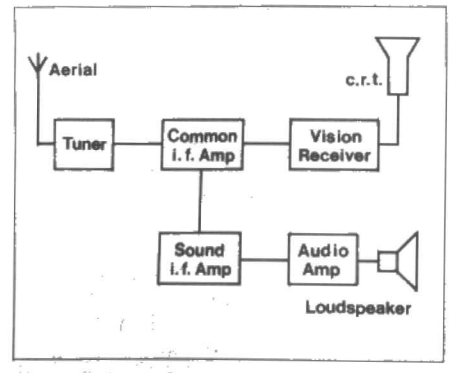


Figure 6. Basic television receiver with quasi-parallel sound.

signal is extracted at intermediate frequency (32.948MHz carrier). The stereo audio outputs from the digital processing are connected to the audio amplifier inputs via the volume controls in the usual way. Electronic switching between digital and f.m. mono sound will be normal.

The Digital Decoder

The stages of digital processing in the decoder are shown in Figure 8. The sound i.f. amplifier is similar to a conventional f.m, i.f. and limiter, but the QPSK demodulator is quite different. These have already been developed in IC form for the Japanese DBS system.

Spectrum Shaping Filter

This filter affects the noise-immunity of the receiver, and for best performance the combined effect of this filter and the corresponding one at the transmitter should be that of a band-pass filter with a −3dB frequency offset of 135kHz, a zero response beyond 364kHz offset and a cosine-squared roll-off. Ideally, too, each of the filters should contribute equally, so the ideal receiver filter would have the response shown in Figure 10.

DQPSK Decoder

One practical DQPSK decoder, for recovering the modulation, is shown in Figure 9, and the stages are described below. The complexity of this device shows why manufacturers are not keen on developing their own devices when the existing Japanese devices can be used.

Modulators

These resolve the incoming carrier into in-phase and quadrature components with respect to the recovered carrier. Resolving on two axes eliminates phase error of the recovered carrier, and allows the output components to be used directly for the following stages without phase tweaking.

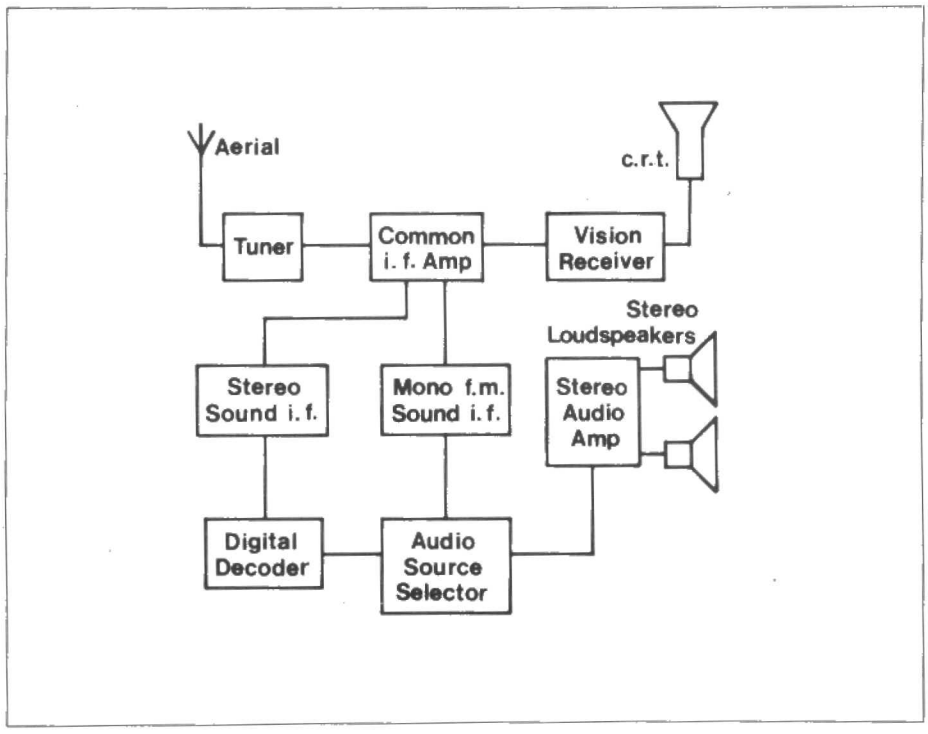


Figure 7. Adding the digital decoder.

Carrier Recovery

This is achieved by means of a phase-locked loop and a voltage-controlled crystal oscillator (VCXO). Because the carrier component of the signal may be absent during certain data sequences, a logic matrix effectively restores the carrier component by intermodulating the sidebands.

Data Slicers

These slice the data signals between set amplitude limits, thus converting the noisy, more or less sinusoidal pulse signals to flat-topped pulses with jittery edge transitions. By incorporating a.g.c., the slicers can adapt to variations in input signal level.

Clock Recovery

This is basically another phase-locked VCXO running at a multiple of the bit-rate, and it produces a clean square-wave at bit-rate, 728kHz. Dividing this by 2 gives a symbol-rate clock for the phase-detectors. The differential decoder and the parallel-to-serial converter also need clock signals.

Differential Decoder

Since the modulation is differential, in order to recover a symbol it is necessary to compare each pair of

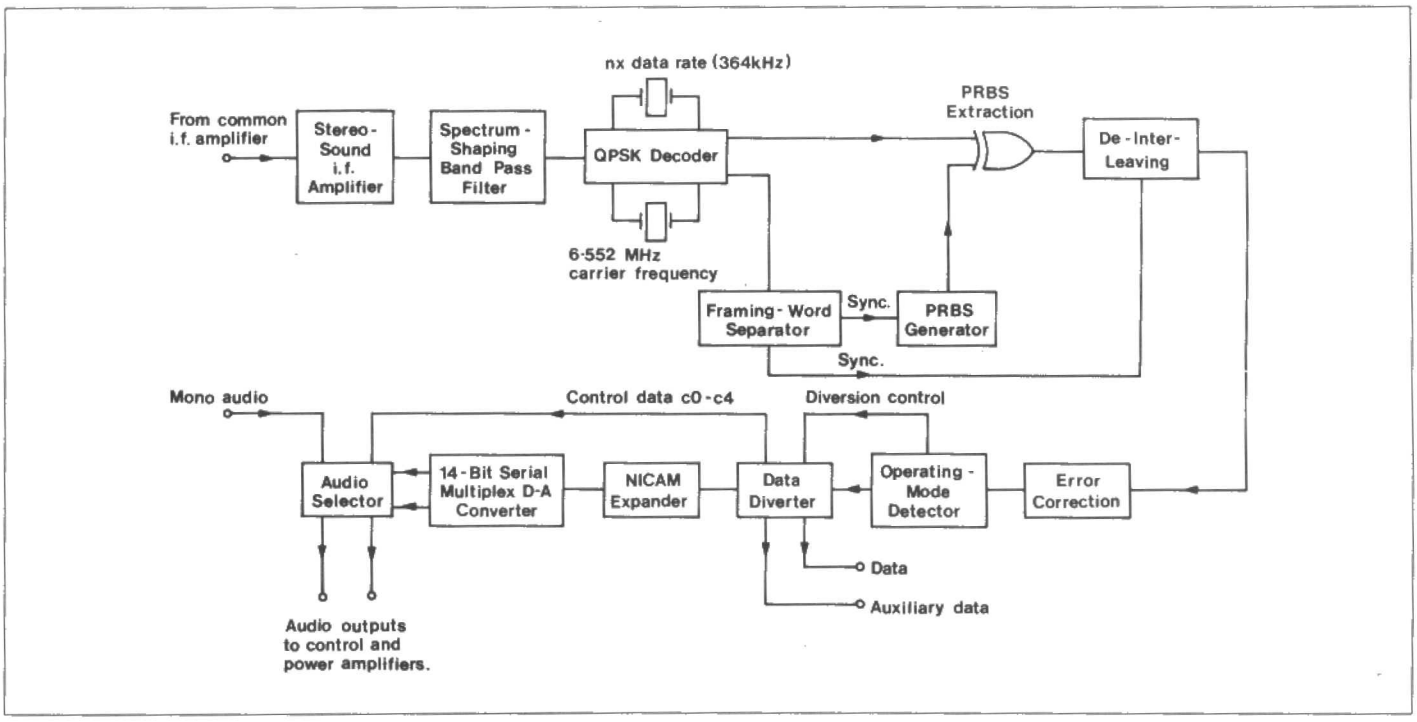


Figure 8. Block diagram of the digital decoder.

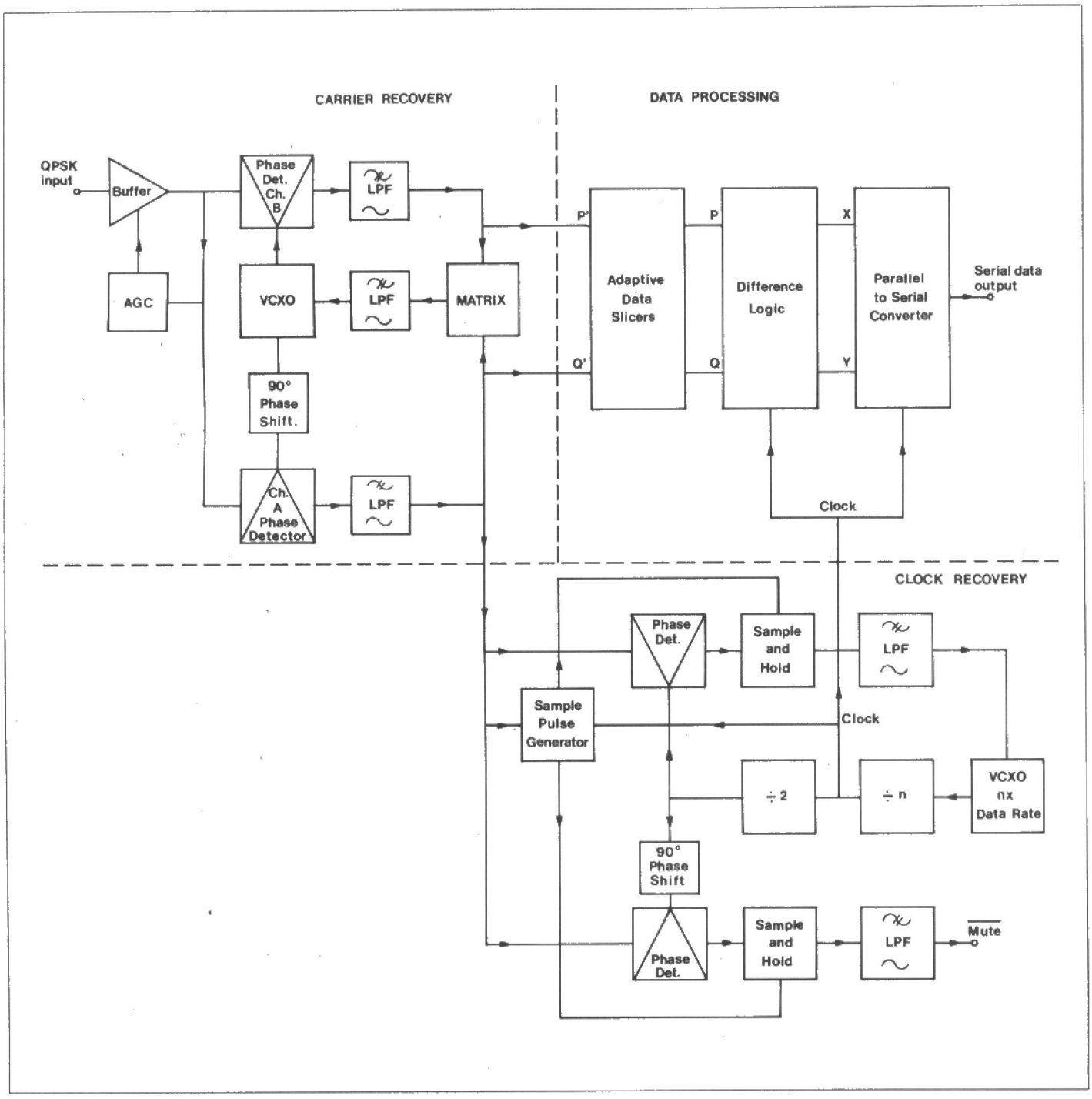


Figure 9. QPSK decoder.

symbols from the data slicers with the previous pair, using D-type flip-flops or the equivalent as temporary stores.

2-Bit Parallel-to-Serial Converter

This is a standard building-block, which in principle is a two-way switch driven at bit-rate, looking at each symbol alternately.

Frame Synch Word Detector

This is also a standard function, which can be achieved with an 8-bit serial register and an 8-input exclusive-OR gate.

Pseudo-Random Binary Sequence (PRBS) Subtractor

The energy-dispersal PRBS for this system is $2^9 - 1 = 511$ bits long, and there-fore runs through about one and a half times in the 720 bit period between

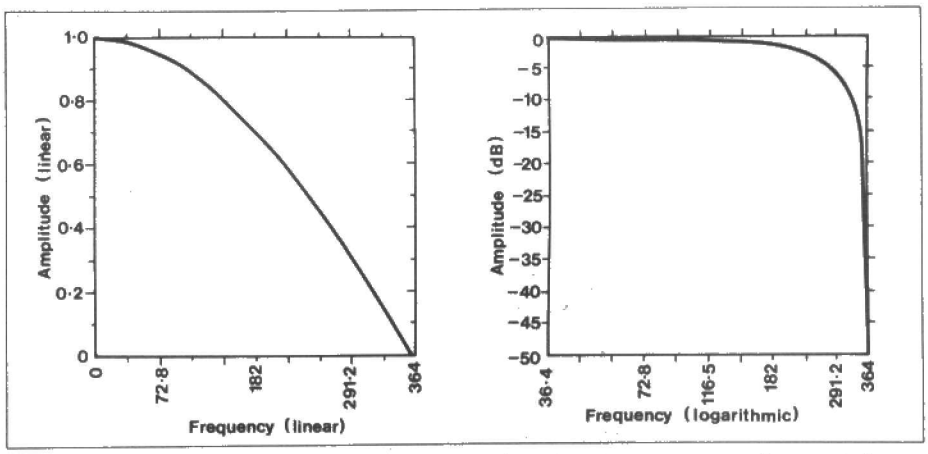


Figure 10. Receiver band-pass filter. Plotted on linear scales, the response can be seen to be shaped like the first quarter of a cosine curve. On the more usual decibel/logarithmic scales, it can be seen to have a very steep cut-off. The attenuation at and beyond 346kHz should be infinite. The filter at the transmitter should be identical in response.

frame alignment words. The generator is synchronised to the framing word by loading the shift-register with 'all-1s' and starting the register clock pulses after the last bit of the frame alignment word. The generator output is then serially subtracted from the bit-stream by means of an exclusive-OR gate (in principle), as shown by the truth-table in Figure 11.

De-interleaving

This function is similar to that in CD-players, and uses what is in effect a dedicated computer to re-arrange the bits.

Error Correction

The error-correction process is very complicated, and cannot be dealt with in detail. While not the same as Compact Disk error-correction, it is possible to use some of the IC's developed for CD to do the error-correction for this system.

Operating-Mode Detector and Data Diverter

The detector looks at the control bits C0 to C4, and determines what configuration the data diverter and audio selector should adopt. The data diverter may or may not have outputs for the auxilliary data and main-channel data, whose purposes have not yet been defined.

NICAM Expander

This reverses the compression process by using the scale-factor bits and the inverse of the compression rules to reconstruct 14-bit signals. There may be feedback of higher-level error-correction data to the earlier error-corrector, or a second stage of correction may follow the expander.

Digital-to-Analogue Conversion

This is by far the most well-known step in the whole process, and can also be carried out by IC's developed for Compact Disk.

As an alternative to converting the stereo audio signals to analogue at this point, it should be possible to put them into a form compatible with the ITT Digivision sound chips, so that volume, tone, balance and stereo base-line enhancement can all be carried out digitally.

Chip-Set and Receiver Development

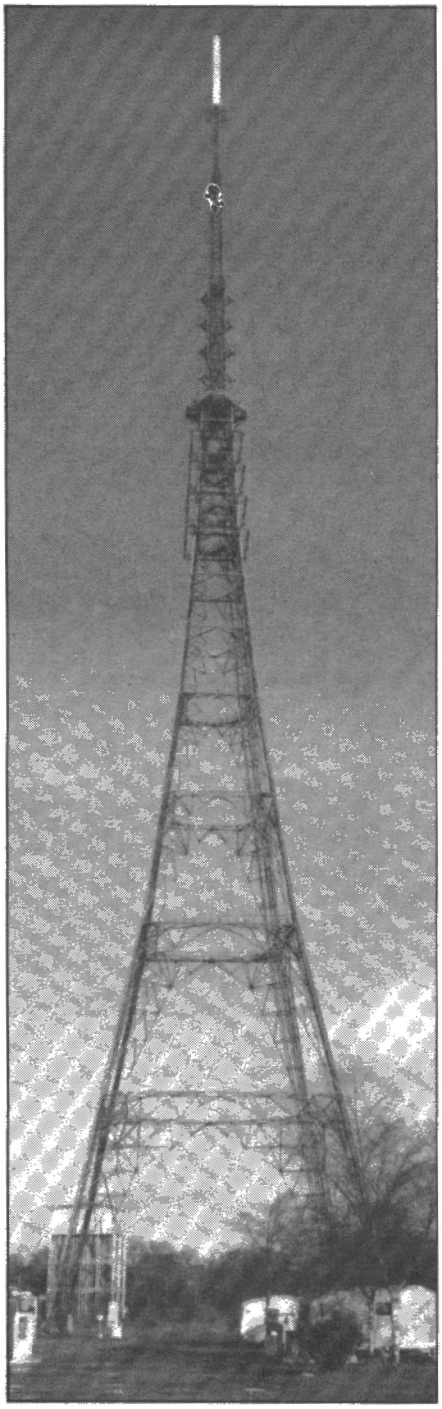
There are now about nine companies manufacturing TV's in Britain, two and a bit of which are British-managed at top level. Thorn-EMI-Ferguson have developed their own chip-set for all the processing between the QPSK demodulator output and the DAC's, and these are being made by Texas Instruments. While TEF may offer them eventually to other setmakers, this will probably not happen for at least 1 year. Meanwhile, Philips-owned Mullard are developing devices for those parts of the decoder that existing CD chips will not reach. Both of these companies will use existing QPSK demodulator chips, presumably Japanese.

A = audio data
TP = PRBS at transmission end
T = transmitted signal
RP = PRBS at receiving end (synchronised with TP by frame alignment word)
R = recovered audio bits (should be identical to A)

A	TP	T = A ⊕ TP	RP	R = T ⊕ RP
0	0	0	0	0
0	1	1	1	0
1	0	1	0	1
1	1	0	1	1

⊕ means 'Exclusive OR'

Figure 11. 'Addition' and 'subtraction' of the pseudo-random binary sequence (PRBS) using exclusive-OR gates.



Both Hitachi and Toshiba let it be known within the industry that they intended to launch receivers this year, even about now, but subsequently changed their minds. Any receivers which are made available will receive the programmes which are now being broadcast on a daily basis. These are not advertised in programme schedules for fear of causing confusion, as the 'stereo' receivers on the market (which will reproduce stereo from an audio source, such as VCR), are not fitted with NICAM 728 decoders.

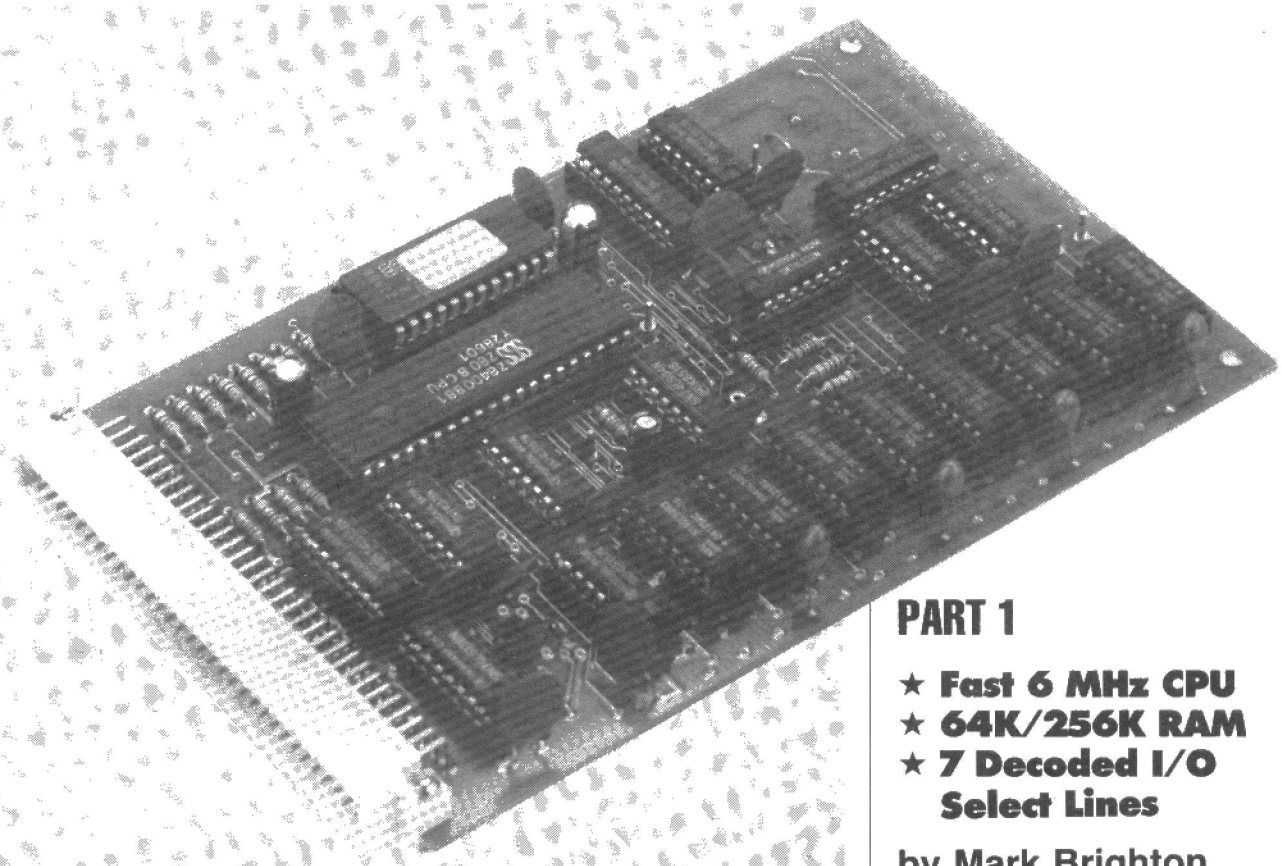
Conclusion

We have seen how the problems of providing a stereo sound system for TV broadcasting have been overcome by the use of advanced digital technology. Time was when the signal-processing required for f.m. stereo was considered complicated! While not much detail can be given yet about receiver designs, because of the fierce competition and the need to protect patent rights, it is clear that there will be receivers available for all who want the new service, with the prospect, too, of on-going innovation through the introduction of new data services, etc. to keep up the demand for new receivers. This will counteract the effect on sales volume of the very high reliability now achieved in TV sets, which implies a working life of around 20 years for a receiver made today. To stay even in its present unhealthy (low profitability) state the receiver industry requires each TV to be thrown away (not sold or used in the bedroom) after five years' use, (or a 20% increase in retail prices, perhaps!).

We stopped our analysis of the receiver at the low level audio stages. What will happen to these high-quality digital signals after that? All that remains, of course, is to push them through 2W amplifiers into 'huge' 3 inch elliptical (side-facing?) speakers, as in current receivers. Or do you think that better power amplifiers and loudspeaker systems will be fitted to real stereo TV's? Has it happened with CD tower systems? Will things ever change? Well, they might. The increasing sophistication of consumer electronic products is provoking more enlightened design engineers to strive for more equal levels of performance in each functional block of the system. But they are naturally still vulnerable to the irresistible challenge of making their designs ever cheaper.

Acknowledgements

Much of the material for this article was of necessity extracted (not copied!) from BBC Research Department Reports, and the official system specification, together with other published papers. Considerable help was also received from Thorn-EMI Ferguson Ltd. at Enfield and Bradford, from the BBC Engineering Information Department, and from Mullard Limited.



FRAME STORE

PART 1

★ **Fast 6 MHz CPU**
★ **64K/256K RAM**
★ **7 Decoded I/O Select Lines**

by Mark Brighton

Z80-B CPU CARD

This article describes the first part of a modular Z80 based micro-controller system, designed to meet the needs of a wide range of control monitor and display applications, where it is often not desirable to dedicate a home micro to a single task. Some applications for the system will be presented in future issues of "Electronics", the first being as part of a video display for WEFAX weather satellite pictures, received by the "Mapsat" Receiver/Decoder System, described in previous issues.

Two expansion modules are under development at the time of writing, a parallel/serial I/O card using the Z80 SIO and DART peripheral chips, and a high resolution graphics card using the Yamaha/Microsoft V9938 MSX graphics processor. These modules will be connected to the Z80B CPU card by means of a common motherboard, the whole system being in eurocard format.

The modules themselves will be equipped for expansion, being supplied as a basic kit, with optional extra parts to bring them up to full capability. In this way it is hoped that the system may be tailored by the user to suit his/her particular application (and finances!), without the built in redundancy that often results from using 'off-the-peg' computers (high resolution colour graphics and six octave polyphonic sound are a little excessive for a central heating controller or a home security system!).

The CPU card described here is no exception to the expandable concept just out-lined, being supplied in basic form as a 'bare bones' minimum computer circuit which forms the foundation module of

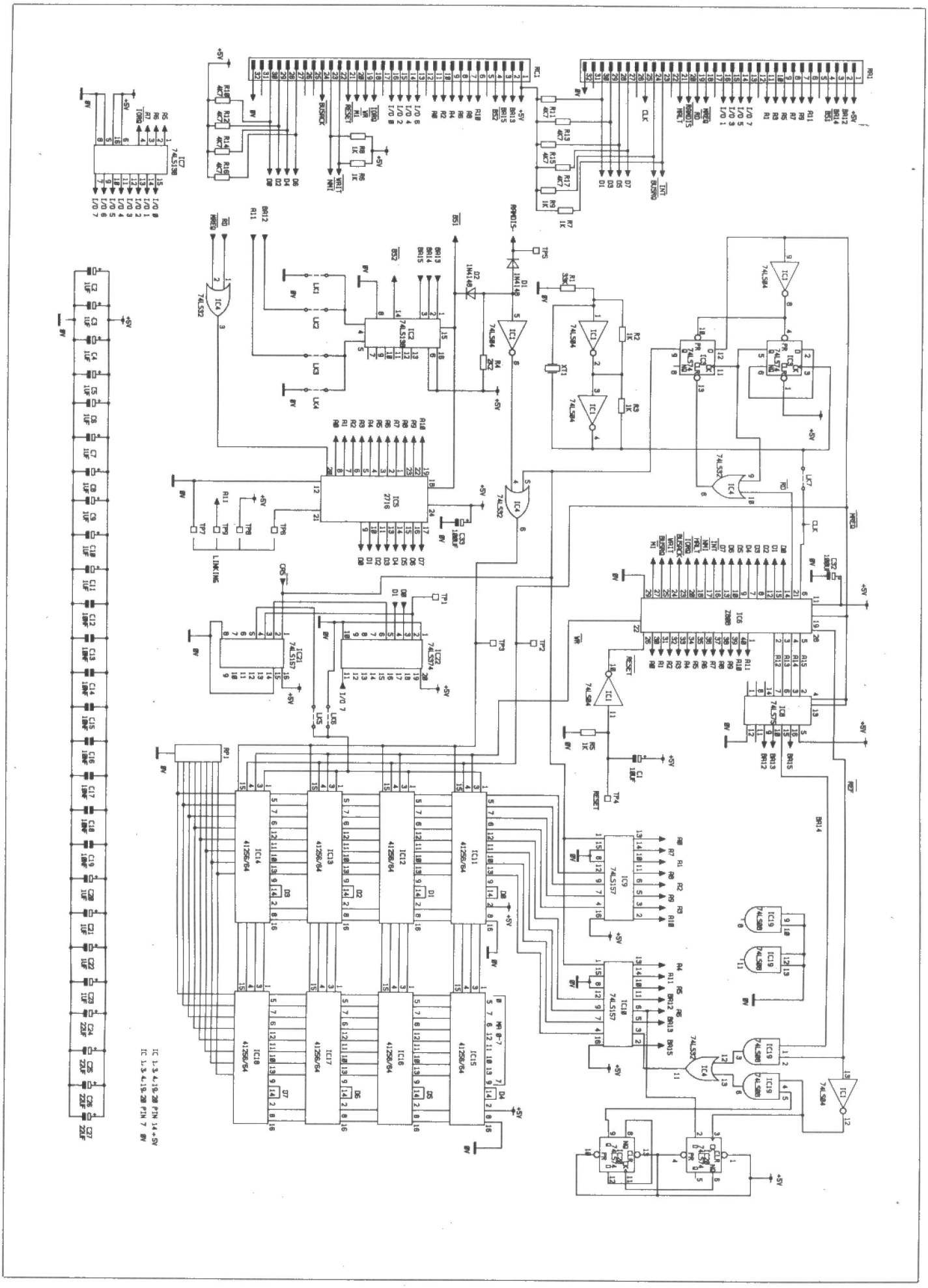


Figure 1. Circuit Diagram.

any dedicated system built up by the addition of a combination of expansion modules. Optional parts for this board consist of a number of logic chips which provide all the multiplexed address and refresh circuitry for dynamic RAMs, with linking options to enable the use of 64K or 256K DRAMs. The operation of these circuits will be covered at the end of the following basic circuit description.

NOTE: Only the basic kit is required for the WEFAX Frame Store.

Circuit Description

The heart of the circuit, shown in Figure 1, is a Z80B CPU chip (IC6) running at 6.144MHz, which makes it half as fast again as its older brother the Z80A, still to be found in many popular personal computers. The clock circuit is formed by inverters IC1a and IC1b, R1, R2, R3 and XT1, and provides a system clock on the edge connector, as well as clocking the column address strobe (CAS) generator IC3 (if fitted). If an external system clock signal is available, Link 7 may be omitted and the external clock connected to the system clock pin on the edge connector (PA1.25). This should be a single phase square wave clock with a 50/50 mark/space ratio. RESET for the processor (and any other boards connected to the system) is provided via inverter IC1e by RC network R5/C1. An active high reset signal may be input on reset pin TP4 to Cold Start the system.

The four most significant address lines out of the processor (A12-A15) are buffered by IC8, a dual two bit transparent latch clocked by the Memory Request (MREQ) line from the CPU. The buffered products BA12-BA15 are taken to an address decoder chip IC2, which provides two memory mapped ROM select lines BS1, starting at $0000 and BS2 starting at $2000. These blocks may be 2K, 4K or 8K long, depending on the positions of links 1 to 4 (see Table 1).

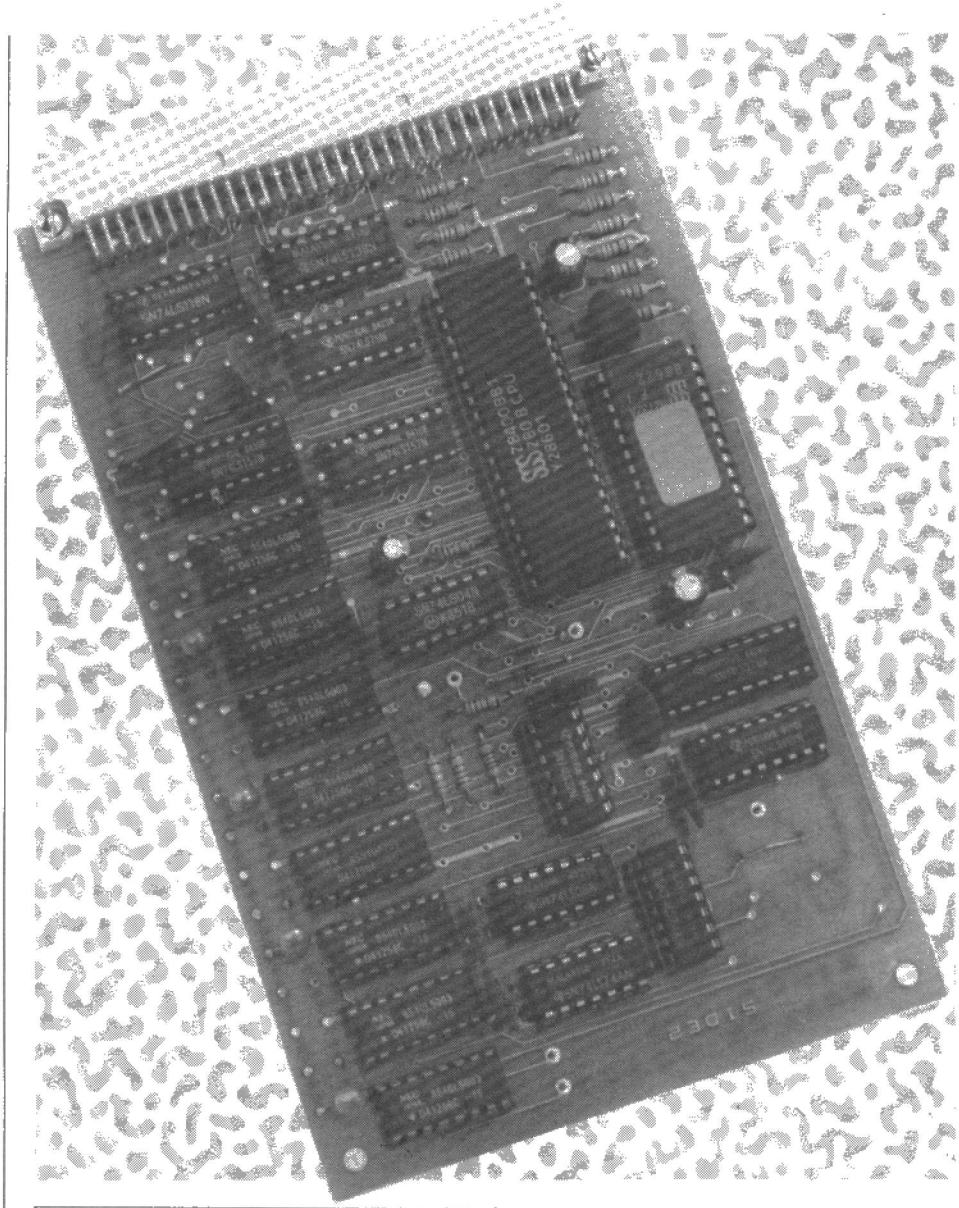
NOTE: If an external ROM/RAM is to be enabled by BS2, the RAM disable line (RAMDIS) should be connected to BS2 to avoid contention on the data bus (BS1 is already so connected, being used to enable the internal ROM).

The internal ROM position IC5 is a 24-pin standard 'byte-wide' pin-out and will accept single rail 2716 or 2732 EPROMs. When buying ROMs for this board, bear in mind that they will have to have an access time less than or equal to 250ns when running the system at the maximum clock speed of 6.144MHz. In practical terms this may mean that it is not possible to use a 2716 at full clock speed, since it is usually only available up to about 350ns access time, but as the board will function quite normally at any clock speed less than maximum, some lower speed applications will suit the 2716 ROM's less frantic way of life admirably.

	LINK			
	1	2	3	4
2K	×	√	√	×
4K	×	√	×	√
8K	√	×	×	√

√ = Fit Link × = No Link

Table 1.



OPTIONS	LINK		
1.	TP6	—	TP8
2.	TP6	—	TP7
3.	TP6	—	SWITCH*
4.	TP6	—	TP9

*See Text

Table 2.

The function of IC5, pin 21, varies depending on the type of ROM fitted, and several strapping options have therefore been provided (see Table 2). For the sake of clarity I will summarise the options provided as follows:

1. When using a 2716 EPROM pin 21 (Vpp) should be connected to +5V during normal use.
2. If using a 2732 for reasons of speed alone, where less than 2K of space is needed for the control program, pin 21 (A11) may be linked to 0V and Links 1 to 4 wired to select a 2K ROM. Only the low half of the ROM is then used, which results in an extra 8K of RAM being available if 256K DRAMs are fitted, since the ROM overlays the first 2, 4 or 8K of each 64K block of RAM. This is unavoidable, due to the 64K address range of the Z80, and the need to have the control program accessable to the processor at any time, regardless of which block of RAM is selected.
3. When using a 2732 for programs less than 2K in length, it is possible to treat the two halves of the ROM as separate "SUBROMs", as follows. Two separate programs are developed and burnt into the EPROM along with their jump vector tables if required. The first, in the lower half of the ROM, is jumped to by means of the cold start vector, at address $0000, in the normal way. The second program is burnt into the upper half of the EPROM, from ROM address $1000 onwards. The

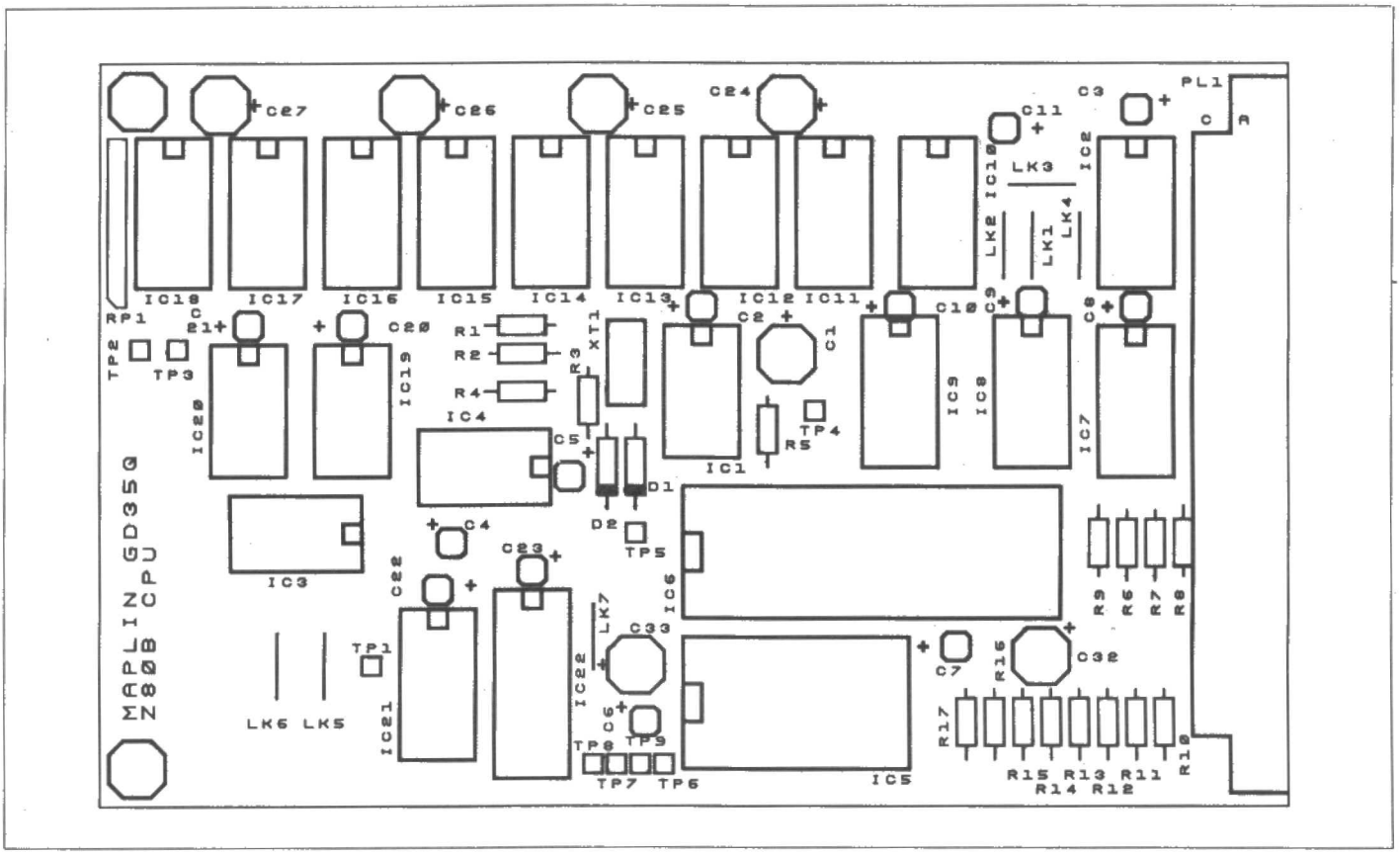


Figure 2. PCB Layout.

program is written to run from address $0000 however, including the duplicate jump vector table starting at ROM address $1000. Pin 21 on the EPROM is then wired to the centre pole of a SPDT toggle switch whose outer contacts are wired one to 5V and one to 0V. Whichever half of the ROM is selected by this switch will slot into the first 2K of the memory map, and run on power up. In this way the CPU board may fulfill two completely different functions at the flick of a switch, or run two different versions of the same program for different conditions.

4. The last option is simply to wire pin 21 on the 2732 to the processor A11 line, and select a 4K space with Links 1 to 4. This allows for up to 4K of control program/data.

The Z80 architecture allows the first 256 addresses to be used as I/O ports to control or monitor external devices. It is the common practice to interface all peripheral devices to these special I/O locations, thereby leaving the maximum space available in the memory map for ROM/RAM. IC7 decodes these addresses into eight I/O block select signals (I/O 0 - 7, active low) which may be used to enable external peripheral devices. Each block is 32 bytes long, so devices which have a number of addressable internal registers can be connected to a number of address lines (A0 - A4) to I/O map the individual registers. IC7 is enabled by the I/O request (IOREQ) line from the processor, as opposed to the usual Memory Request control line, in order to locate any devices selected by it in the I/O map instead of the memory map.

NOTE: If 256K DRAMs are fitted, I/O7 is used to enable the memory block select circuitry, and is not, therefore, available for external use.

The DRAM support circuitry consists of several stages having the following interrelationship:

Access to a memory location within a static RAM is accomplished by presenting the chip with a parallel binary address, and enabling the chip by means of a block select pulse, which is directly compatible with the information coming from the processor. Dynamic RAMs, however, are not arranged as a long linear sequence of locations, but as a two dimensional matrix. They therefore require a two part address to access any one location, a row address and a column address. To further complicate matters, both addresses are input on the same set of inputs to reduce the pin count of the chip, so separate row and column address strobes have to be derived to clock the addresses into the DRAMs. In this design, the processor MREQ signal provides the row address strobe (RAS) and IC3, a dual D-type flip/flop, along with IC1d and IC4c, derives the column address strobe (CAS) from MREQ, CLK and RD. The length of the CAS pulse depends on whether the access to RAM is a write cycle or a read cycle, CAS starting later for write cycles to prevent the DRAMs placing data on the bus at the same time as the processor. The CAS signal is gated to the DRAMs via IC4b, which blocks the CAS signal during ROM access, thus preventing the DRAMs from responding to a READ in the ROM address space. Row and column addresses are formed by splitting the address bus into two groups, the eight least significant bits being presented during RAS time, and the most significant during CAS time via multiplexer chips IC9 and IC10.

Dynamic RAM chips must be accessed at certain periodic intervals in order to retain their contents. This process is called 'refresh' and the Z80 has a built in refresh control line to simplify the refresh circuitry required. The refresh mode chosen for this circuit is called 'RAS Only Refresh', which requires that all rows be accessed within the stipulated refresh period (in the case of the 41256 DRAM refresh cycle time is 4ms maximum). Fortunately the Z80 has a built in refresh counter which generates the row addresses, places them on the bus when it is otherwise unused, and outputs a pulse on the refresh line, so it would seem that little or no external circuitry would be required. Unfortunately, since the basic design of the Z80 is getting a little long in the tooth, the refresh address is intended for the older generation of DRAMs, which only required a six bit refresh address as opposed to the current generation which requires a seven bit address. This limitation is overcome by using the top bit of the Z80 refresh counter to clock an external one bit counter formed by IC20, a dual D-type flip/flop. The output of this counter, (FA7), is switched in to replace

BA14 during refresh time by IC1f, IC19a, IC19b and IC4d.

NOTE: If using the WAIT input to interface slow peripherals etc. it should be noted that refresh of DRAMs will cease for as long as WAIT states exist in the processor. Use of BUSRQ will have a similar effect.

If 64K DRAMs are fitted, no block switching of RAM is necessary, so IC21 and IC22 may be omitted, and Link 6 wired in to select 64K RAM. Where 256K DRAMs are used, Link 5 should be fitted. Fit only Link 5 or Link 6, not both! IC22 is an eight bit latch, I/O mapped between $E0 and $FF. The two least significant bits of data written to this port determine which RAM block is slotted into the memory map (%XXXXXX00 to %XXXXXX11). This Block Select Address is then multiplexed onto the DRAMs' MA8 line by IC21.

Construction

Before commencing construction of this unit, read the Constructor's Guide which accompanies the kit. Referring to the pcb legend and Parts List, insert and solder all resistors, capacitors and IC sockets. Special care should be taken to ensure that no short-circuits are created whilst soldering, especially around the IC sockets. Links should now be fitted as required; these are described in Tables 1 and 2. Link 7 should also be fitted if using the 6.144 MHz internal clock.

Bolt the 64-way edge connector into position on the pcb, and solder the pins onto the board. Fit all ICs carefully into their sockets noting correct orientation. This completes assembly of the unit.

For reference purposes, Figure 3 shows the functions of the 64 pins on the edge connector.

Testing and Use

Those of you who are building this project as part of the WEFAX Satellite Display System need not worry overmuch about this section, unless you have access to a Z80 assembler and EPROM programmer, and are particularly interested in getting to grips with the working of the system. The Frame Store Project will include a ROM which will contain a program to input and display picture information from the MAPSAT decoder. This may be used to test the complete system.

It is not practical to test all facilities on a CPU system such as this without specialised test equipment, and/or a huge set of machine code test routines. Therefore the test routine included here in Listing 1 is a simple 'go/no-go' test which, when run, will take the RAM block select line at TP1 alternately high and low, each cycle occurring at (approx.) one second intervals. This may be monitored with a multimeter, oscilloscope, logic probe or a light emitting diode in series with a 470Ω resistor.

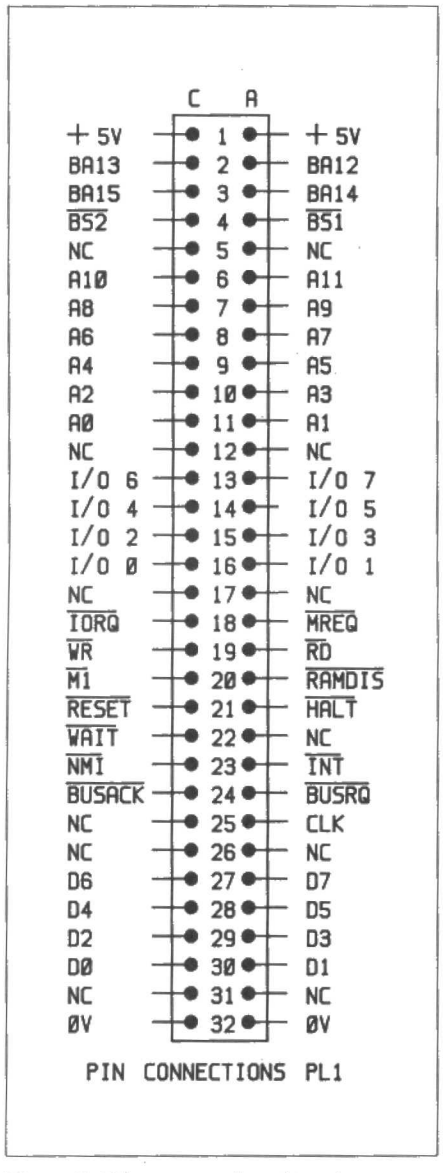


Figure 3. Edge connector pin-outs.

NOTE: This test requires that a 74LS374 is fitted at IC22.

Listing 1 was produced using the Amstrad CPC128 and Hisoft assembler, but it should not prove too difficult to enter the program on any other Z80 assembler system providing the following stipulations can be met.

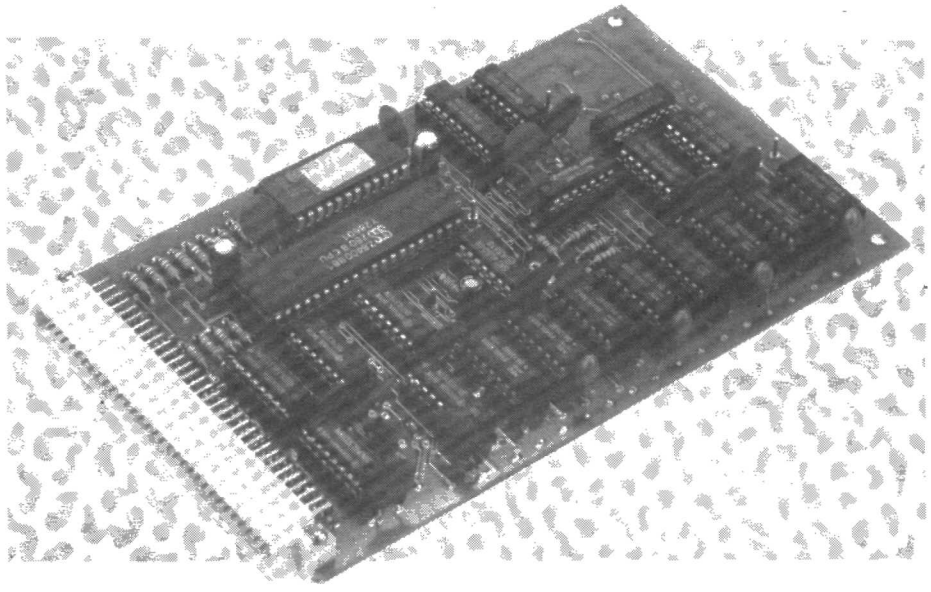
1. The assembler should be capable of assembling programs to run in the first 2K, 4K, or 8K of memory (the host machine will probably have a ROM in this area and it will not therefore be possible to assemble a program to actually reside in it), either to disk or tape or some other area of memory. If this is not possible, the program will have to be manually re-coded to correct jump instructions, etc.
2. Those of you who are not using a full blown development system, with on-board EPROM programming or ROMulation facilities, will know that it can be very tedious entering a hexadecimal version of your program manually on EPROM programmers such as the Softy. This can be overcome on EPROM programmers having an RS232 interface (Softy, Gang-of-eight plus, etc.), by down-loading the assembled program directly into the programmer having first converted the object code file information into a format which the programmer can accept. This obviates the need for much laborious typing, and makes the process of testing and subsequent evolution of programs far easier. Information about the data formats required by the programmers is usually included in the handbooks accompanying them.

```
0100                    10          ORG   #0100
0100                    20          ENT   $
00FD                    30 PORT:    EQU   #00FD
0100  3EFF              40 START:   LD    A,#FF
0102  D3FD              50          OUT   (PORT),A
0104  01FFFF            60          LD    BC,#FFFF
0107  0B                70 LOOP1:   DEC   BC
0108  78                80          LD    A,B
0109  B1                90          OR    C
010A  20FB             100          JR    NZ,LOOP1
010C  3E00             110          LD    A,#00
010E  D3FD             120          OUT   (PORT),A
0110  01FFFF           130          LD    BC,#FFFF
0113  0B               140 LOOP2:   DEC   BC
0114  78               150          LD    A,B
0115  B1               160          OR    C
0116  20FB             170          JR    NZ,LOOP2
0118  C30001           180          JP    START
```

Listing 1.

NOTE: It is not possible to use the ROMulation facilities of some systems on this Z80B card since their slower clock speeds can cause timing problems upon access.

While it is not possible to present any further information about the use of such an open ended system here, application information will be included in this magazine as it becomes available. In the meantime, I would be glad to receive any comments concerning application details or criticism (preferably constructive) developed by readers or users of the system. Application information received may, if of sufficient interest, be considered for inclusion in future issues of this magazine, and should be addressed to myself at the Magazine address.



Z80B CPU CARD PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1	33k	1	(M33K)
R2,3,5-9	1k	7	(M1K)
R4	2k2	1	(M2K2)
R10-17	4k7	8	(M4K7)
RP1	SIL Resistor 2k2	1	(RA28F)
CAPACITORS			
C1	10µF 50V PC Electrolytic	1	(FF04E)
C2-11,20-23	1µF 35V Tantalum	14	(WW60Q)
C32,33	100µF 10V PC Electrolytic	2	(FF10L)
	(Note C12 to C19 on circuit diagram are integral with sockets for IC's 11 to 18)		
SEMICONDUCTORS			
D1,2	1N4148	2	(QL80B)
XT1	6·144 MHz Crystal	1	(FY83E)
IC1	74LS04	1	(YF04E)
IC2,7	74LS138	2	(YF53H)
IC3	74LS74	1	(YF31J)
IC4	74LS32	1	(YF21X)
IC6	Z80B	1	(UF74R)
IC8	74LS75	1	(YF32K)
MISCELLANEOUS			
PL1	PCB Plug	1	(FJ51F)
	DIL Socket 14-pin	5	(BL18U)
	DIL Socket 16-pin	6	(BL19V)
	DIL Socket 20-pin	1	(HQ77J)
	DIL Socket 24-pin	1	(BL20W)
	DIL Socket 40-pin	1	(HQ36R)
	P.C. Board	1	(GD35Q)
	ISO Bolt M2.5x12mm	1 Pkt	(BF55K)
	ISO Nut M2.5	1 Pkt	(BF59P)
	ISO Shake M2.5	1 Pkt	(BF45Y)
OPTIONAL *(not in kit)*			
IC5	2716 for 450ns	1	(QQ07H)
	or 2732 for 350ns	1	(QQ08J)
	or 2732 for 200ns	1	(UH88V)
	In addition to the basic CPU the following RAM extensions are shown below:		
	Decoupled DIL Socket 16-pin	8	(FP79L)
C24-27	47µF 16V Tantalum	4	(WW76H)
IC9,10	74LS157	2	(YF61R)
IC19	74LS08	1	(YF06G)
IC20	74LS74	1	(YF31J)
OPTIONAL: 64K RAM version			
IC11-18	4164	8	(QQ06G)
OPTIONAL: 256K RAM version			
IC11-18	41256	8	(QY74R)
IC21	74LS157	1	(YF61R)
IC22	74LS374	1	(YH16S)

A kit of parts for the basic Z80B CPU is available, excluding optional and extension parts:
Order As LM29G (Z80B CPU Basic Kit) Price £27.95

Some items in the above kit list are also obtainable separately, but are not shown in the 1987 catalogue:
Z80B CPU Card PCB **Order As GD35Q Price £14.95**
EPROM 2732 200ns **Order As UH88V Price £9.95**
Decoupled 16-pin DIL Socket **Order As FP79L Price 68p**

PRIZE DRAW WINNERS

The winner of the star prize, a beautiful Ford Fiesta, was Mr Martin Buzzard from Byfleet in Surrey.

The 100 runners-up who won Digital Alarm Clock Radios are as follows:–

C.F. Newby-Robson, Sawtry; G.T. Brooks, Tunbridge Wells; B. Robertson, Towcester; J. Torselli, Basingstoke; T.G. Lloyd, Hereford; D.A. Harley, Romsey; A.W. Rayer, Edinburgh; M.S. Price, Rickmansworth; A.J. Johnson, Sidcup; B.W. Rodgers, Sheffield; D.A. Hollands, Dorchester; G. Pugh, Stafford; E.B. Beard, Shrewsbury; G. Russell, Polegate; Dr. G.G. Spence, Glasgow; C.P. Norfolk, Penrith; R.J. Green, Chatteris; S. Parker, Leeds; A.J.B. Buchanan, Leighton Buzzard; A. Smith, Broadstone; P.T. Williams, Gillingham; C. Walker, Skellingthorpe; S.P. Randall, Plymouth; M.B. Fraser, Luton; R.W. Gregory, Gt Yarmouth; R. Leborgne, Sittingbourne; C. Abrahams, Brentwood; D.J. Prosser, Swindon; T. Skinner, Hoveton; J.S. Baxter, Letchworth; Dr. M.W. Holmes, Skipton; D. Baldwinson, Altrincham; B.A. Winn, St. Leonards-on-Sea; Dr. J.B.L. Bard, Edinburgh; R.C. Smith, Whitby; B. Mannas, Huntingdon; G. Paviour, Melksham; A.A. Faulkner, Londonderry; R. Dowden, Camberley; P. Bunney, Broughton-in-Furness; R. Stevens, Orpington; A. Stuart, Musselburgh; K. Lord, Luton; A. Willis, Farnborough; S. Sharpe, Headley Down; W.C. Woodhouse, New Barnet; S. Bond, Huddersfield; H.A. Bunn, Lincoln; C.P.L. Fillingham, Benbecula; A. Gilbert, Fareham; P.J. Everest, Thatcham; A.S.A. Issufo, Dewsbury; L. Jurd, Tadworth; B.W. Parkins, Kings Langley; H. Doherty, Castlewellan; Mr. Semple, Holt; N.J. Wadsworth, Broadstone; M. Meswania, Luton; R. Haslehurst, Northwich; D.M. Bull, Nottingham; A. Antoniou, London; D. Howell, Barry; J.P. Brett, Newcastle-on-Tyne; G.R. Pringle, Gt Yarmouth; J. Caulfield, Bristol; G.H. Bradley, Ashford; E.P. Thomas, Cardiff; J. Loughridge, Manchester; K.E. Berry, Penryn; S.A. Fletcher, Abergavenny; C. Gardner, Marlborough; A.C. Hobbs, Welwyn Garden City; P. Teague, Stoke-on-Trent; C.R. Paterson, Glasgow; A. Allen, Manchester; A. Stoddart, Brentwood; P.N. Paterson, Holmes Chapel; J. Scaife, Broughton Astley; C. Espie, Wishaw; M.A. Bond, Godstone; Dr. P.M. Holt, Welwyn Garden City; P.A. Rosbotham, Wigan; A. Hurley, Fareham; A.P. Hume, Hitchin; P.J. Mills, Cannock; H.M. Humphreys, Belfast; A. Fisher, Torquay; D. Greenwood, Bodmin; N. Ray, Ware; B. Goodyear, Oswestry; R. Gould, Weymouth; P. Phillips, Chepstow; K. Sunil, Roehampton; I. Tutin, Thatcham; N.K. Williams, Dunfermline; A. McGhie, Isle of Whithorn; S.R. Hill, Loughborough; J.M.C. Bassett, Nottingham; R.G. Scott, Giffnock; N.J. Dupres, Powys.

TEST GEAR AND MEASUREMENTS

by Danny Stewart
Part 5

In part 4 we saw many different ways in which AC voltage, current and power could be monitored or measured using meter movements operating on electromagnetic or electrostatic principles. Here we examine instruments using more in the way of electronic circuitry.

Electronic Meters

Meters developed from the electro-mechanical with magnetic sensor and needle movement to the fully digital-electronic, i.e. digital display with electronic sensor. In between these two stages there was an attempt at turning the electro-mechanical device partly electronic by using an amplifier to drive the needle. Rather like using a quartz movement in an analogue wrist watch.

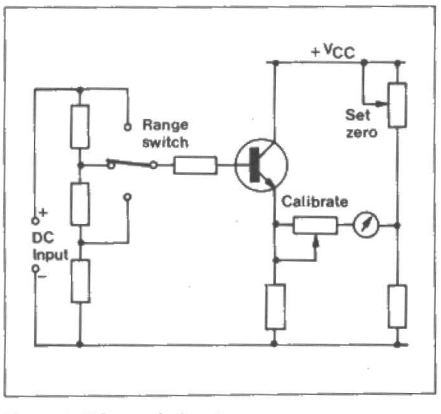


Figure 1. DC coupled meter.

If a transistor is connected as one arm of a bridge circuit, Figure 1, its input can be limited to a safe value by an attenuator and range switch. The attenuator and range switch ensure that the input voltage is limited to a safe value, i.e. the turn on voltage of the transistor. Direct coupled amplifiers however, suffer from drift and a better method of measuring a low value of DC voltage is to turn it into an AC voltage in order to amplify it, then convert it back into DC. In this way, DC voltages of a few microvolt can be measured. Reed vibrators for converting DC into AC are well known where car batteries have been used during power strikes. Here a chopper (vibrator) using photodiodes, will be described.

Figure 2 shows how an oscillator is used to illuminate neon lamps on alternate half cycles. Neon Lamp A then illuminates photodiode B and C and Lamp D illuminates photodiodes E and F. Two photodiodes are required in the input and output to cope with the positive and negative going waveform. Photodiodes have low resistance (hundreds of ohms) when illuminated and high resistance (thousands of ohms) when not illuminated. The photodiodes act as gates, opening and shutting at a rate determined by the oscillator, usually a few hundred Hertz.

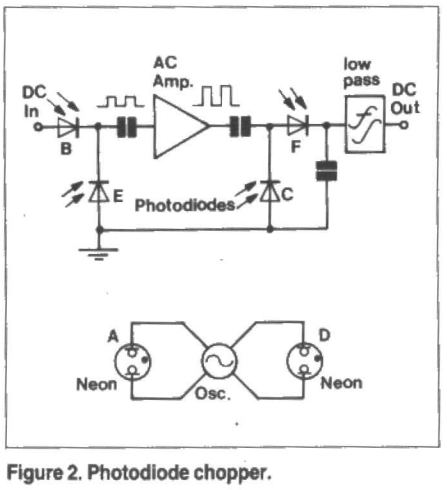


Figure 2. Photodiode chopper.

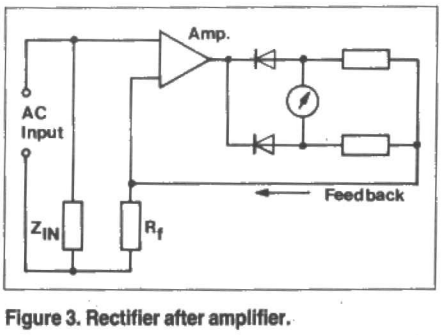


Figure 3. Rectifier after amplifier.

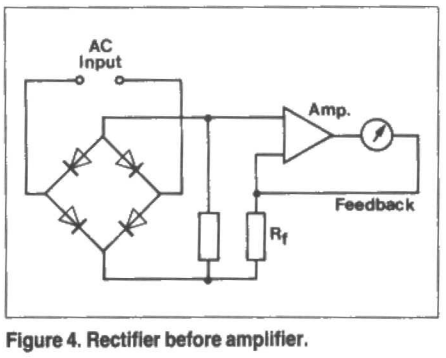


Figure 4. Rectifier before amplifier.

This rate is limited by the photodiodes ability to change states from low to high resistance and back again. Thus when the input is enabled, the corresponding output will be of the opposite polarity taking the phase inversion of the amplifier into account. The higher output voltage is then able to drive the meter needle and of course the scale readings are reduced to compensate for the amplification. The low pass filter in the output removes any AC left in the signal.

As before, in order to measure AC, a rectifier is required. However, there is a choice of putting the rectifier before or after the amplifier. Figure 3 shows that the signal is amplified first, then rectified. In this arrangement there is a requirement for large quantities of negative feedback to compensate for the non-linearity of the diodes. This means that the open loop gain of the amplifier must be large. The full wave rectifier and bridge arrangement in the output is then used to produce a reading.

Alternatively, the rectifier can precede the amplifier, Figure 4, in which case a DC amplifier with zero drift is required. Other rectifier arrangements are possible. Figure 5

shows that a half wave rectifier can be connected to a DC amplifier. Instead of reading the average value of the rectified waveform, there may be a need to read the peak value. In which case, Figure 6 shows a peak rectifier where the capacitor charges to the peak value.

Figure 7 shows a voltage doubler or peak to peak rectifier, and the output is twice the peak value. All the above arrangements apply to sine waves, i.e. a form factor of 1.11. What if the wave is not a sine wave or there are several different waveforms? Then thermocouples must be used to measure the heating effect. This is called an r.m.s. responding meter. But thermocouples are non-linear, so if two thermocouples are connected in opposition, the non-linear effect cancels.

Balanced-Bridge Amplifier

Instead of using a single DC amplifier, two DC amplifiers can be used in a bridge formation such as Figure 8, where T1 and T2 are two arms of a bridge and R1 and R2 the other two arms. Bipolar transistors or field effect transistors can be used as the active devices.

With no DC input, the transistors operate in the OFF region. But since transistors cannot be exactly identical, there will be a slight imbalance, causing current to flow through the meter. Therefore, a zero adjust is useful.

Differential Voltmeters

These use the principle of the potentiometer and are sometimes called potentiometric voltmeters. A potentiometer is a kind of bridge and both use a comparison principle which is highly accurate.

Figure 9 shows a differential voltmeter and an accurate meter is not required since absolute voltages are not being measured but a sensitive meter is required to detect the slightest imbalance. The reference voltage is usually a 2 volt DC laboratory standard or Zener controlled supply. A rectifier is used to convert the DC differential voltmeter into an AC differential voltmeter. The main drawback of a differential voltmeter is the loading effect of the input divider.

Digital Voltmeters

Digital voltmeters can work on different principles, one of which is the successive approximation principle. The principle of

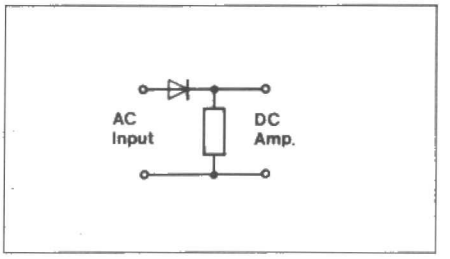


Figure 5. Half wave rectifier.

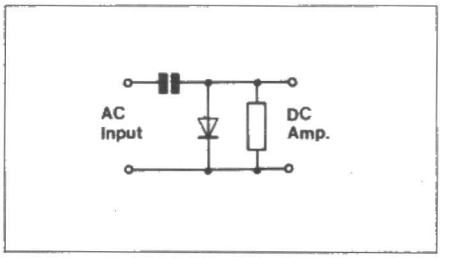


Figure 6. Peak rectifier.

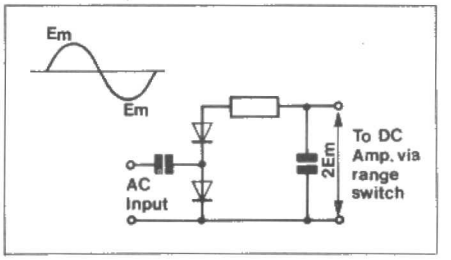


Figure 7. Voltage doubler.

working is illustrated in Figure 10. Suppose a voltage of 9.5V is to be measured, the start/stop multivibrator of Figure 11 sets the D/A converter output to half the reference supply. If this is less than the input voltage a digital one is retained as the most significant bit in the control register. Subsequent voltages are half the previous value and these are compared with the residue from the input. If they are greater than the residue they are rejected. If they are less than the residue, they set the subsequent bits in the control register which then illuminates the digital display.

If the voltage being measured is not a DC voltage, then the input will change constantly. To overcome this a sample and hold circuit is used. The sample and hold circuit can be thought of as a switch and capacitor. The switch is closed whilst sampling the voltage, and open in the hold mode. During the hold period, the voltmeter gets a chance to discharge the capacitor and work out the level of voltage.

Another method of digitally reading an input voltage could, strange as it may seem, employ a servo-controlled motor. Since this method does not read the input in steps like other methods, it is sometimes called the continuous balance method. The reason for this is because the servo-controlled motor tries to balance the input against the reference, continuously. This low cost instrument is about 0.1 per cent accurate and the mechanism takes about two seconds to settle. The chopper is a mechanical device (vibrator) for converting DC to AC. The AC out of the chopper and into the amplifiers is a square wave whose amplitude depends on the difference in amplitudes and polarity of the inputs to the chopper. The servo motor turns in a direction to cancel this difference, and in so doing turns the wheels of the digital readout. The digital readout is a drum type mechanical device.

The most obvious method of measuring an incoming voltage electronically is to generate a ramp and look for coincidence with the incoming voltage. A ramp voltage may be positive going or negative going. Figure 13 shows a negative going ramp, i.e. one that falls towards zero or even below zero.

Let us say the input voltage is coincident with the ramp at point X, and at point Y the ramp has dropped to zero. Therefore the time interval X to Y has to be measured, and this interval has to represent the amplitude of the voltage under measurement. The whole operation represents an analogue to digital conversion since the final display is digital.

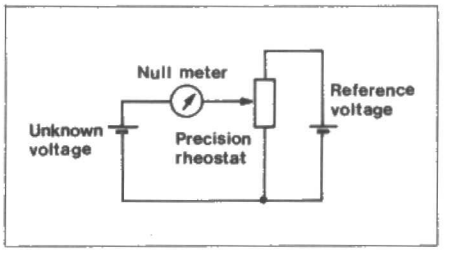


Figure 9. Differential voltmeter.

Input	Volts generated	Input residue
9·5V	8V (Keep)	1·5V
	4V (Discard)	1·5V
	2V (Discard)	1·5V
	1V (Keep)	0·5V
	0·5V (Keep)	0

Figure 10. Successive approximation method.

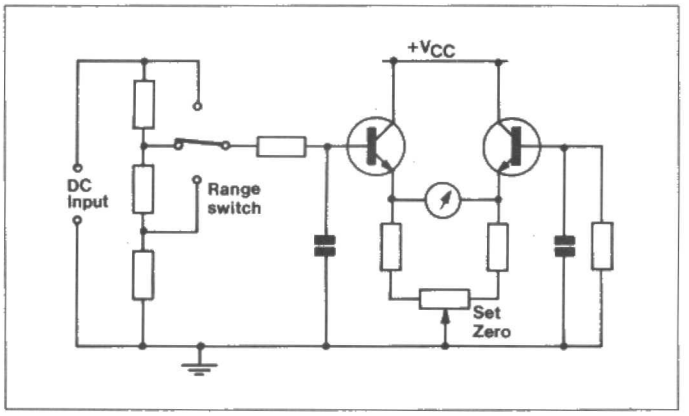


Figure 8. Balanced bridge DC amp.

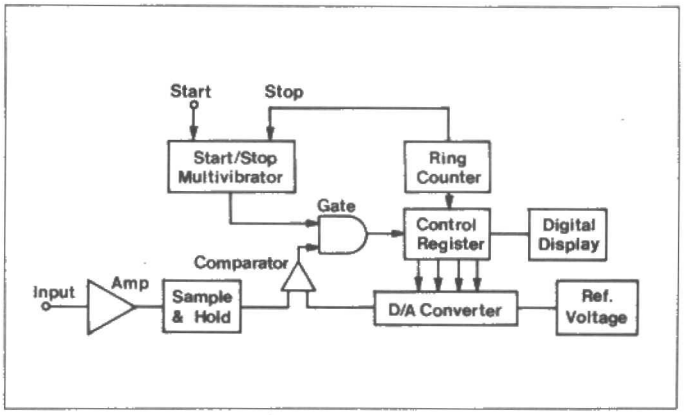


Figure 11. Successive approximation circuit.

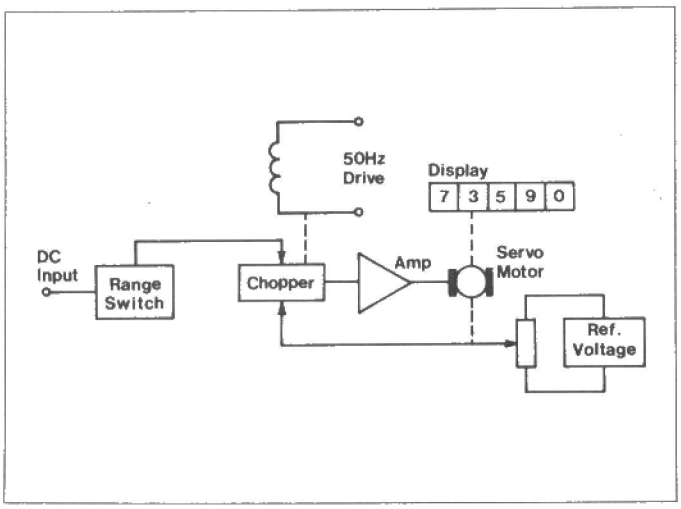


Figure 12. Servo controlled voltmeter.

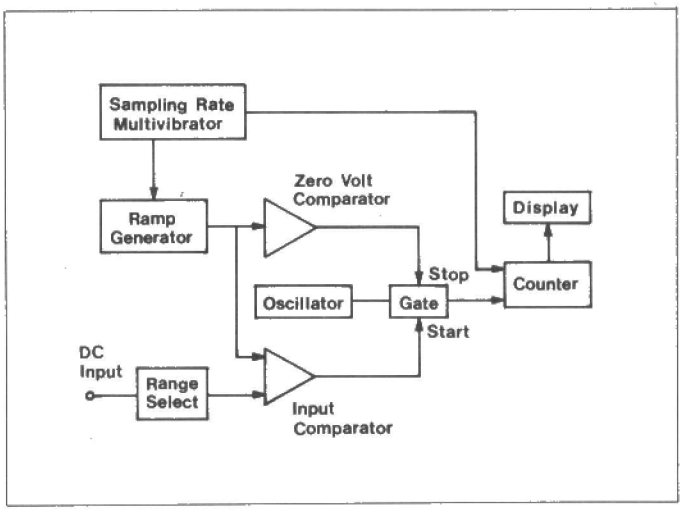


Figure 14. Ramp type digital voltmeter.

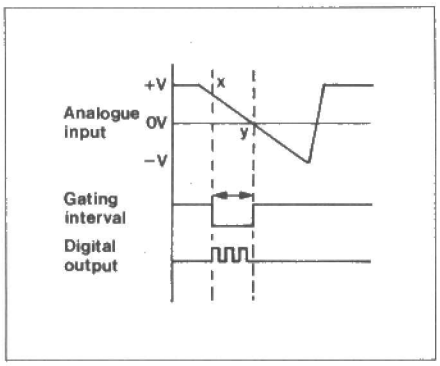


Figure 13. Analogue to digital conversion.

Figure 14 shows a block diagram of a ramp type digital voltmeter. If a start pulse opens the gate of the counter as soon as coincidence is detected, and a stop pulse closes the gate of the counter as soon as the ramp reaches zero, the count can be made to represent the amplitude of the voltage under measurement.

The sampling rate can be carried out by a multivibrator in order to start the next ramp voltage and also cancel the previous display. The rate is adjustable from a few Hz to several kHz. The display can be prevented from 'blinking' by outputting a reading only at the end of each count.

The main types of digital voltmeter examined here are based on the following principles:

Successive Approximation.
Continuous Balance.
Ramps.

In general, digital voltmeters have input ranges of 1 volt to 1000 volts with a good resolution, e.g. 1μV can be measured on the 1V range. The input capacitance is about 40pF and the input resistance 10M ohms.

These instruments are usually accurate to ±0.005% with a stability of 0.008% over half a year.

Electronic Counters

The basic building blocks of an electronic counter are:

a) Multivibrators (flip flops).
b) Logic gates to control the counting periods.
c) A timebase for increasing the frequency or time intervals.

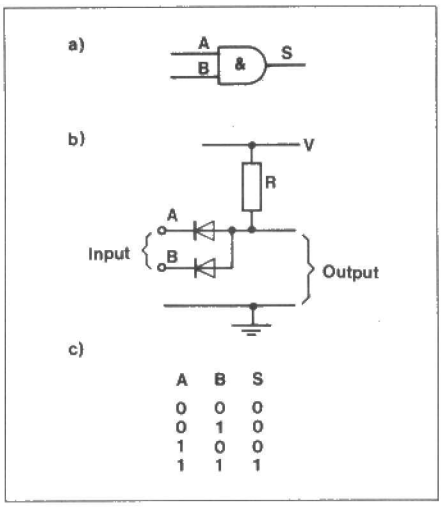


Figure 15. AND gate (a) symbol, (b) circuit, (c) truth table.

Logic Gates

Before going into detail about how such a counter does its input sampling let us undertake a quick revision of logic gates. The basic logic operations are: AND, OR, NOT.

Figure 15a shows the symbol for an AND gate, and Figure 15b the circuit. There is an output only when both inputs are activated. Figure 15c gives the truth table.

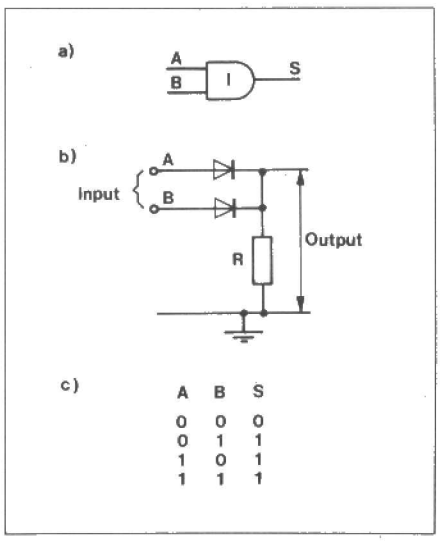


Figure 16. OR gate (a) symbol, (b) circuit, (c) truth table.

Figure 16a shows the symbol for an OR gate. Figure 16b gives an output when either of the inputs are activated, according to the truth table of Figure 16c.

An important logical operation is the NOT gate or inverter, since it is sometimes important to invert a pulse before applying it to subsequent logic gates. An inversion is achieved quite simply by a transistor. Since the output is 180° out of phase with the input, a positive going pulse applied to the input will appear as a negative going pulse at the output. Figure 17a shows the symbol for a NOT gate, and Figure 17b gives the circuit and Figure 17c shows the truth table.

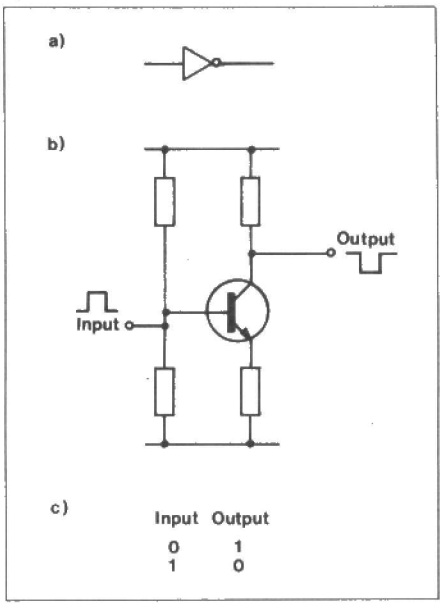


Figure 17. Inverter or NOT gate (a) symbol, (b) circuit, (c) truth table.

Timebase

Since the accuracy of a counter depends on the frequency generated internally, it is important that this frequency is stable. For this reason, the oscillator is usually enclosed in a temperature controlled oven. Just as a television receiver requires a timebase to sweep the screen at regular intervals, a counter requires a clock to open and shut the gates at regular intervals. In addition, the counting period needs to be increased or shortened depending on the frequency of the input.

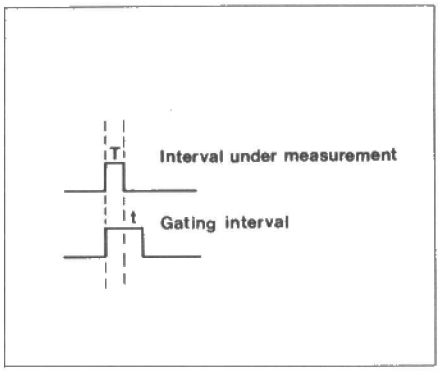


Figure 18. Gating pulse verses period.

It's no use trying to measure a time interval of T, if the gate shuts in interval t, Figure 18. Alteration of the sweep, and hence the gating intervals, is achieved by decade divides. The clock rate, say 10MHz, can be divided by ten successively to give the required rate by a front panel control.

Multivibrators

There are three types of multivibrators; the stable (free running), the monostable (one stable state) and the bistable (two stable states). Here we shall be concerned only with the bistable.

Figure 19 shows an emitter coupled bistable. Let us assume that transistor TR1 is conducting, and that the collector of TR2 is only slightly positive relative to the supply rail, or for practical purposes it is at supply potential. The base of TR2 is therefore at zero potential, and the current through TR1 causes a voltage drop across R7, keeping TR2 cut-off.

In this condition, the potential divider formed by R2, R4 and R6 keeps the base of TR1 negative, i.e. forward biased. This means that the circuit is stable with TR2 cut off and TR1 conducting. To reverse the situation to TR2 conducting and TR1 cut off, a positive trigger pulse is applied to the base of TR1, driving the base-emitter junction to cut-off. At cut-off, the collector of TR1 is at supply potential. This in turn forward biases the emitter-base junction of TR2, via R3, forcing it into conduction. With TR2 conducting, its collector drops to zero volts, therefore the base of TR1 is at zero volts and cut off. The waveforms at different points in the circuit are

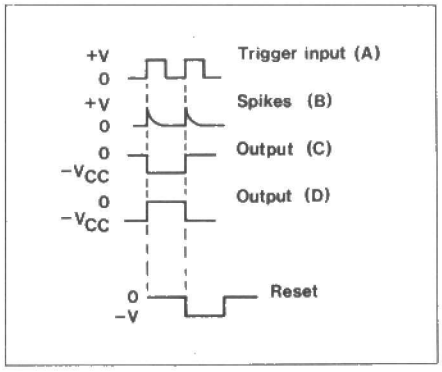


Figure 20. Bistable waveforms.

shown in Figure 20. Notice there is only one output pulse for every two input pulses and the circuit divides by two. Since it works to the base 2, it is a binary counter.

The diode assists in this by removing the negative going spike in the differential waveform. If the diode were not present, the negative going spike would switch on the transistor that was cut off and both transistors would change states. Therefore there would be an output pulse for every input pulse. C1 and C2 are commutating capacitors since they speed up the transition. To ensure that TR1 is on and TR2 off, a reset terminal is provided. If a negative pulse is applied to this terminal, TR1 conducts and TR2 switches off.

Binary Counter

A symbol for the above 'flip-flop', as it is known, circuit is shown in Figure 21. A positive trigger has no effect on the transistor that is cut-off, it only affects the transistor that is on. In order to count in binary, several of these flip-flops can be connected in cascade, as in Figure 22. The output of the conducting transistor is used to trigger the next stage. How this circuit is used to divide successively by two is shown in the waveform diagram of

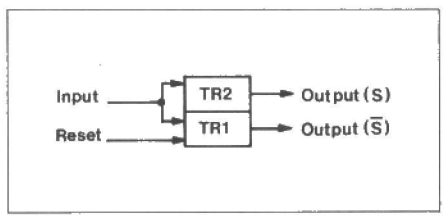


Figure 21. Flip-flop symbol.

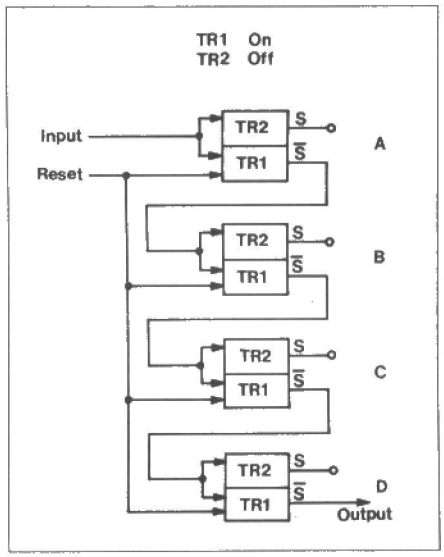


Figure 22. Binary counter.

Figure 23. Another way of representing this is using Table 1. Stage A divides by 2, stage B divides by 4, stage C divides by 8 and stage D divides by 16. This counter counts up to $16(2^4)$ in binary, therefore an 'n' stage counter will count up to 2^n.

Decimal Counter

We ten fingered humans don't find it easy to count in binary, therefore some means has to be devised of converting the binary counter into a decade counter. This is achieved by

Input Pulse	Stage D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

Table 1. Binary counter truth table.

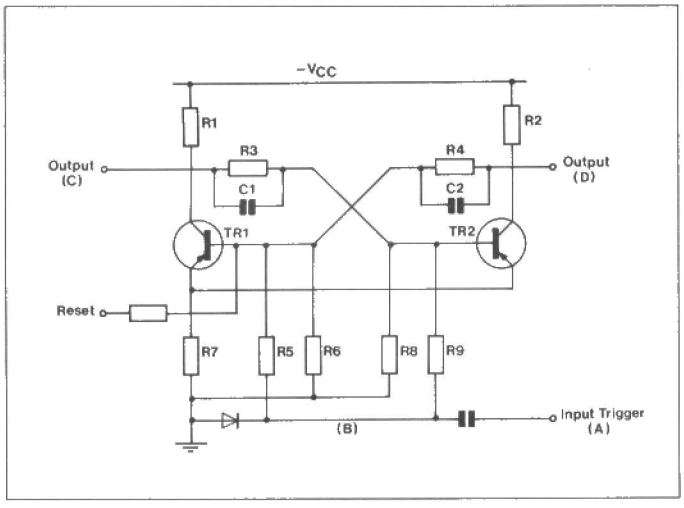


Figure 19. Bistable multivibrator.

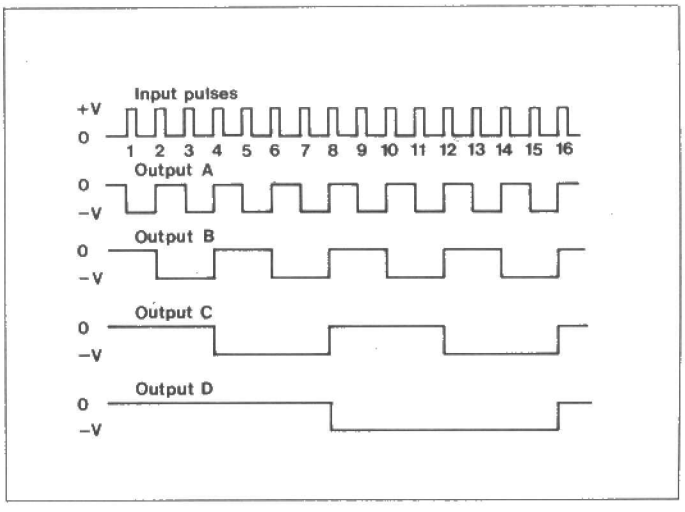


Figure 23. Binary counter waveforms.

feedback and advancing the count by 6 at some stage in a binary counter. The most common commercial decade counter uses four flip-flops as before with feedback as shown by the dotted lines of Figure 24. The corresponding waveforms are shown in Figure 25. At the fourth trigger pulse, stage B is switched on again, advancing the count by 2. At the sixth input pulse, the count is advanced by another 4, giving the required advance of 6. The next four input pulses bring the count up to 10 and all the stages are reset, ready to begin another cycle.

It is useful to compare this diagram with that of Figure 23 to see how feedback prevents the switching off of stages B and C, thereby advancing the count. That is, the stages are controlled by the feedback and ignore the input pulses during these periods.

Universal Counter/Timer

A universal counter/timer usually has facility for two inputs, A and B, and, as in an oscilloscope, one of the signals can act as a trigger for the other. Internal triggers can also be selected. These triggers can be AC or DC voltages for activating the timebase. If an AC waveform is chosen then the triggering can be carried out on the positive or negative slope, Figure 26. This choice improves the stability in counting and displaying the count.

A function switch helps select frequency or period depending on whether one wants to measure the frequency of a signal or the period of one cycle of a waveform. A timebase multiplier switch is a rotary switch which assists the above measurement by expanding or compressing the scale. The decimal point on the digital display is adjusted automatically.

A good machine will also have a memory switched on or off by a slider switch. In the memory mode, the instrument makes one count of the frequency (Hz) or period (seconds) and displays it. With the memory off, the instrument counts and displays

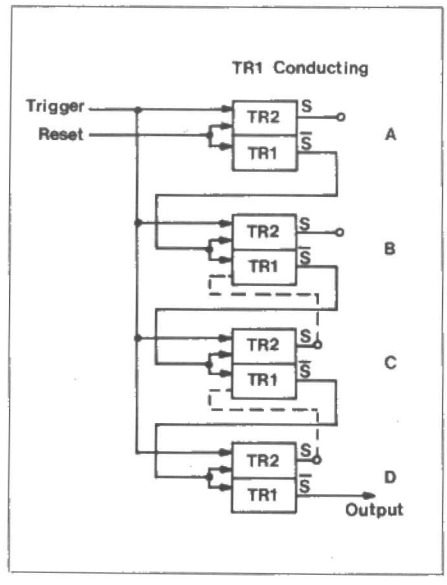


Figure 24. Decade counter.

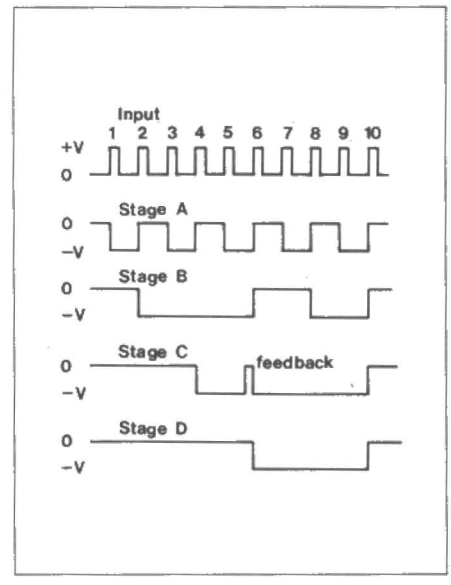


Figure 25. Decade counter waveforms.

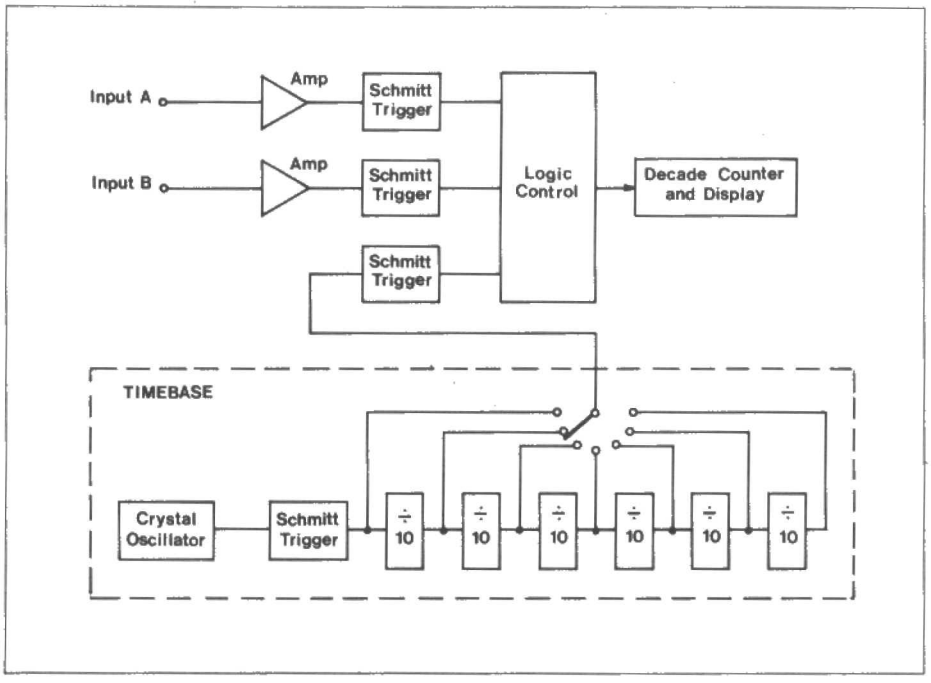


Figure 27. Block diagram of universal counter-timer.

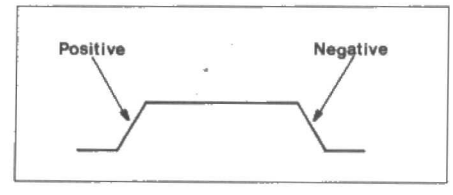


Figure 26. Positive and negative trigger.

continuously, and the display flickers as the count proceeds. A signal lamp marked 'Gate Count' also flickers continuously, except in the memory mode when it stops flashing at the end of a count. Therefore, in the memory mode, a reset button is required if a further count is required. The advantage of the memory mode is that one does not have to watch the display all the time. A block diagram of a universal counter-timer is shown in Figure 27.

Frequency Measurement

This can be described as the number of occurrences in one second. Therefore, if a gate can be opened for one second during which time the input signal can pass through and activate a counter, then the frequency

can be displayed. Figure 28 shows how a gate would open and shut to measure 10 cycles in one second or 10Hz.

Figure 29 shows how this would be implemented using an AND gate to combine the input with the gate open signal. The Schmitt trigger converts the input signal to a square wave which is then differentiated to produce sharp spikes for gating purposes. The space between the spikes is of course the same as that between occurrences of the original waveform.

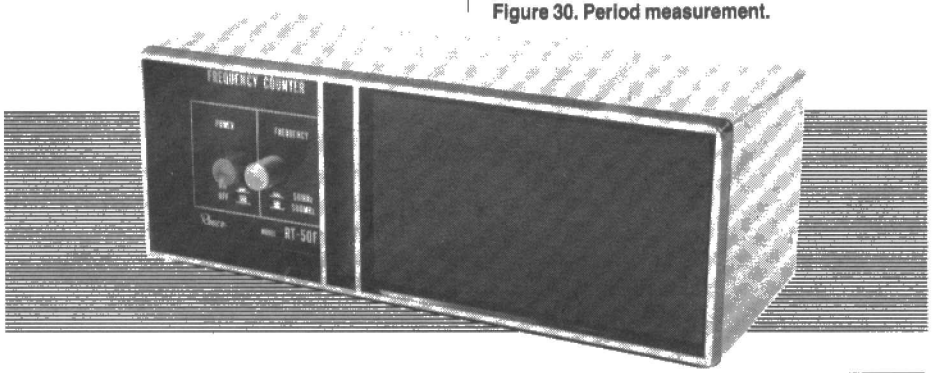
The timebase waveform is also applied via a Schmitt trigger for the same reason. A timebase of 1MHz produces spikes 1μs apart. This can be altered by the multiplier switch to give larger periods up to 1 second.

Period or Time Interval Measurement

In frequency measurement we are interested in the number of occurrences in one second. In period or interval measurement we are interested in the time taken for one occurrence. Therefore, with reference to Figure 30, if a Schmitt trigger starts a counter counting on the positive slope and another Schmitt trigger stops the counter on the negative slope, the counter reading gives the period or time interval. Assuming the time base is 1MHz, then the period would be measured in microseconds. Since the counter is counting in intervals of 1μs, the lowest period that could be measured is 1μs. A waveform shorter than 1μs would require a faster timebase, see Figure 18.

Sources of Error in Counters

The internal oscillator may not be calibrated, and this can be accomplished by tuning it to one of the standard frequencies broadcast over very low frequency radio (VLF) or a frequency transmitted by landline from one of the frequency standards. In England, it is Rugby radio station or by landline from Kingsway, London. Also, a portable instrument that is switched on and off



a lot of the time may take a while to settle down. Long term stability may also be affected since the crystal in the oscillator is under stress continually. This causes bits to flake off the surface, leaving a thinner crystal which gives an increased frequency.

Another source of error is in the gating of the input. Since the gating pulses are not synchronised with the input pulses, the count could be out by one. Consider Figure 31, the interval between pulses is the same for both

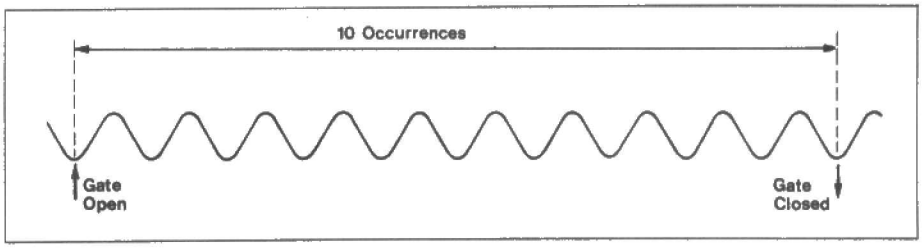


Figure 28. Occurrences in 1 second.

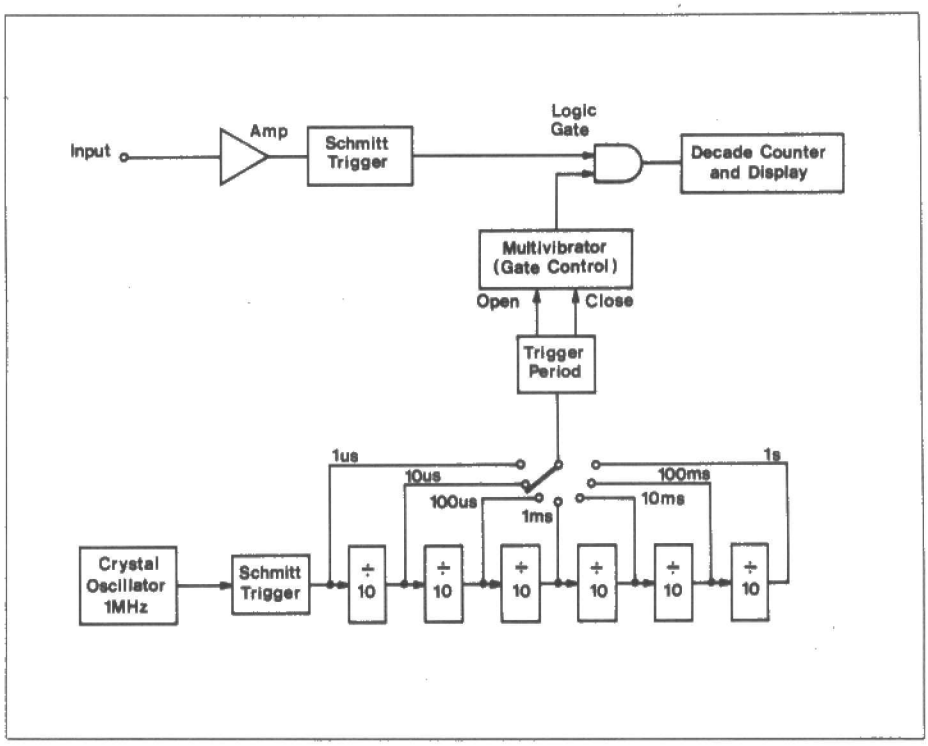


Figure 29. Frequency measurement mode.

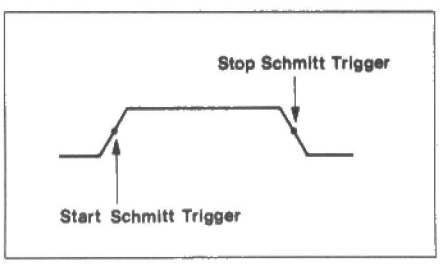


Figure 30. Period measurement.

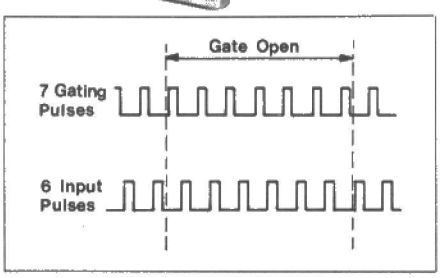


Figure 31. Error in gating.

the gating pulses and input pulses, but because the two signals are not synchronised, only six input pulses have been counted instead of seven. Therefore, at the low frequencies, a count can be out by as much as 10%, and period measurements are better than frequency measurements. The frequency can then be calculated from the period measured:

$$\left(f = \frac{1}{T}\right)$$

The crossover point between frequency and period measurements can be derived:

Let fi = internal frequency of the instrument
fx = unknown signal

The number of pulses counted in a period measurement: P = fi/fx

If the gate is set at 1 second, then the number of pulses counted in a frequency measurement: F = fx.

The crossover occurs when:

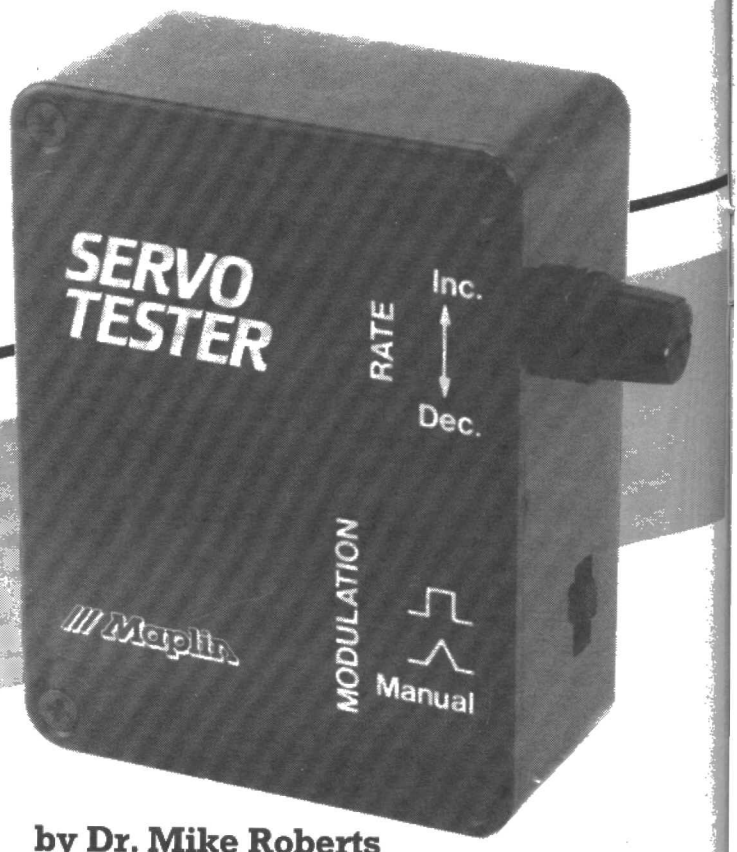
$$P = F$$

$$\text{or } \frac{fi}{fx} = fx$$

That is $fx = \sqrt{fi}$

The crossover is at the square root of the internal clock. So if the clock frequency is 1MHz, the crossover is at 1kHz. Below this frequency, period measurements are more accurate and above this, frequency measurements are better.

SERVO TESTER



★ Two Automatic Check Modes.
★ Manual Switch Incorporated.
★ Checks Servo Travel, Sensitivity, Transit Times and Overshoot.
★ Simple Construction.

by Dr. Mike Roberts

This tester has been designed to measure the performance of servos and aid fault finding. It allows manual adjustment of the servo output and has two automatic modes. In the first automatic mode the output signal is slowly changed from one end of the range to the other and back again. This tests the slow response of the servo (regulator response). The speed of change is adjustable from about 0.2 seconds to 50 seconds for full travel. The second automatic mode switches the output signal from one end of the range to the other. This tests the fast response of the servo (servo response). The time between switching is adjustable over the same range as in the first automatic mode.

The signal that has to be generated is a train of positive pulses each of length between 1ms and 2ms at a repetition rate (frame) of 20ms. A 1ms pulse represents one end of the servo travel, and a 2ms pulse the other. Pulses in between these values drive the servo proportionally between the two extremes.

Circuit Description

The circuit is shown in Figure 1. It is built up from three sections. These are: the frame generator, a voltage controlled pulse width generator, and a waveform generator.

The frame generator centres around IC1b and c. This is a standard CMOS

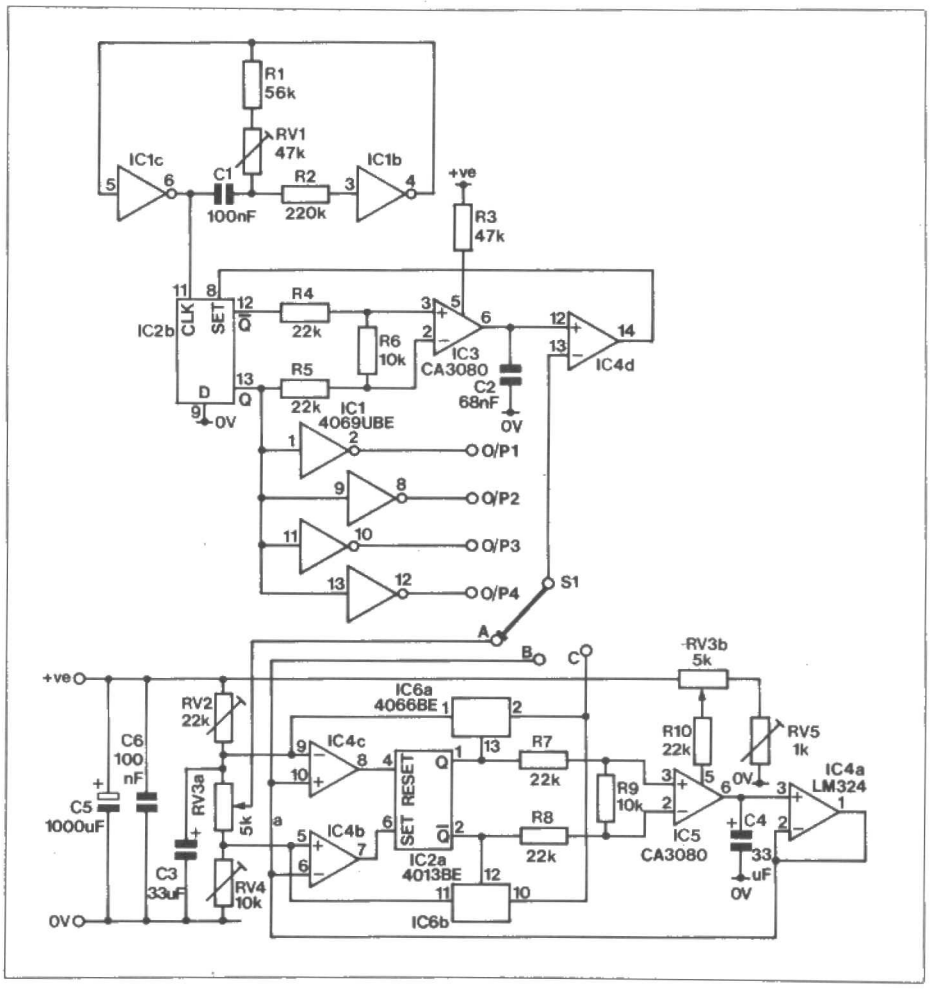


Figure 1. Circuit diagram.

oscillator circuit. It generates a square wave with a frequency which corresponds to the desired 20ms frame. The frame length can be adjusted by RV1. However, this adjustment is not critical, as will be seen later, and those without access to timing equipment can happily leave RV1 in its mid-position.

Both the pulse generator and the waveform generator use the CA3080 operational transconductance amplifier to generate triangular waveforms. This amplifier is similar to conventional operational amplifiers except that it is the output current rather than the output voltage that is proportional to the difference in input voltages. Also, the gain of the amplifier is set by the current allowed into pin 5 (amplifier bias current). The amplifier responds linearly for input voltage differences up to 0.1V. At this point the maximum output current is achieved. This maximum current is equal in magnitude to the amplifier bias current.

A ramp waveform can be generated by applying a fixed current to a capacitor. The rate of rise is governed by:

$$\frac{\text{Voltage (V)}}{\text{Time (s)}} = \frac{\text{Current (A)}}{\text{Capacitance (F)}}$$

A triangular waveform can be generated by alternating the direction of the fixed current. The CA3080 is a convenient device to use to achieve this. By alternating the input voltage differential from +1V to −1V, the output current is at the maximum (saturation) level (equal to the amplifier bias current) and the direction alternates with the polarity of the input.

Now back to our circuit. The pulse generator produces pulses of width between 1 and 2ms. The length is governed by the input voltage (from the waveform generator), and the repetition rate is governed by the frame generator.

IC3 is the CA3080 operational transconductance amplifier. IC4d is a voltage comparator, and IC2b is a 'D' type flip-flop. In its idle state Q is high (5V) and $\overline{Q}$ is low (0V). Hence IC3 is trying to discharge C2. However, when C2 is completely discharged it can go no further and it sits close to 0V. When a rising edge is received into the clock input of the flip-flop, the Q output is set equal to the 'D' input, i.e. 0V. Conversely, $\overline{Q}$ flips to 5V. This gives a positive voltage to IC3 and it starts charging C2. Initially the voltage on C2 is lower than the control voltage. Hence the output from IC4d is low (0V). The voltage on C2 rises at a steady rate set by R3 and C2. When this voltage exceeds the control voltage, the output of IC4d goes high (5V). This immediately 'SETS' the flip-flop, i.e. Q = high (5V), $\overline{Q}$ = low (0V). This in turn reverses the input to IC3 and C2 starts to discharge.

The time that Q is low is set by the rate of rise of the voltage on C2 and the control voltage. The rate of rise of the voltage on C2 is fixed. Hence the length of time that Q is low is proportional to the control voltage. The output from Q is inverted and buffered by IC1a, d, e, and f, so that up to four servos can be driven at once. Overall then, the output pulses are of length governed by the input voltage and the repetition rate is set by the frame generator. The various waveforms are shown in Figure 2.

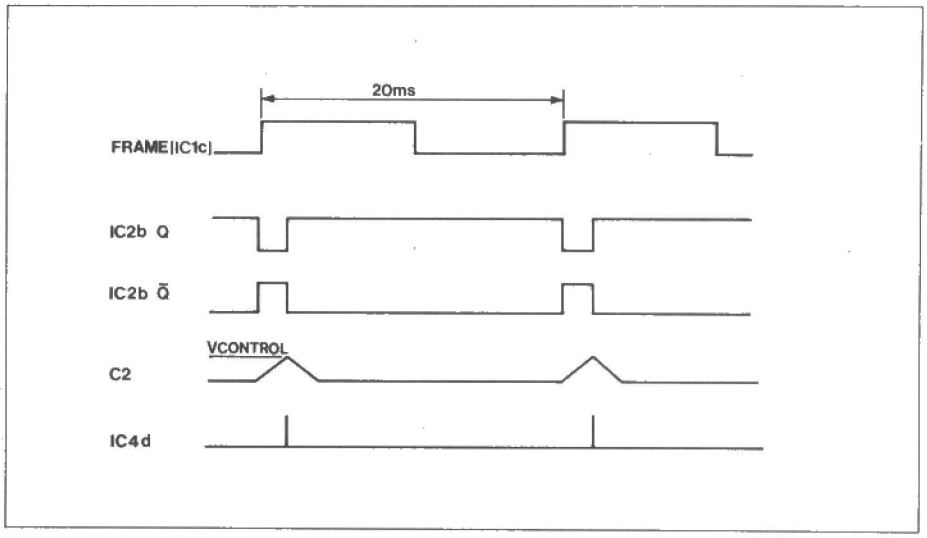


Figure 2. Waveforms.

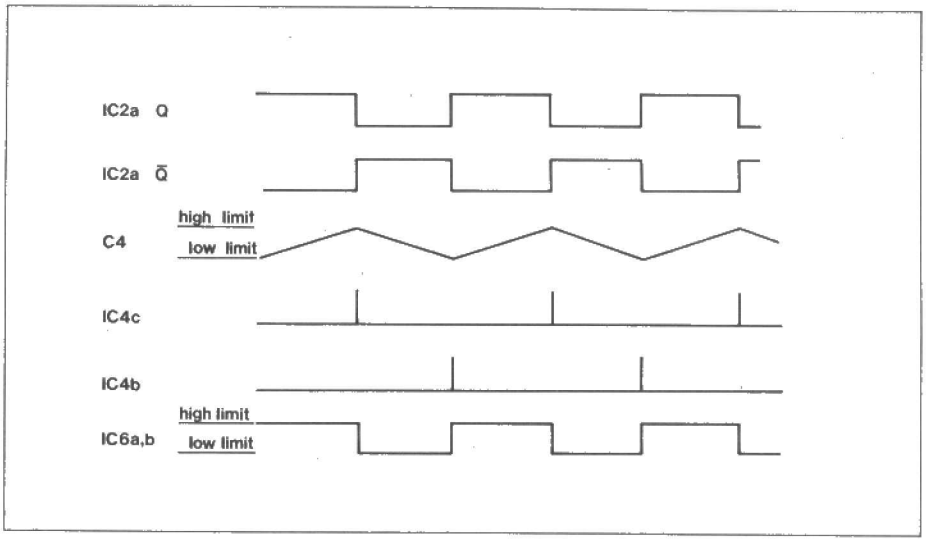


Figure 3. More Waveforms.

The waveform generator produces one of three outputs. These are all generated at the same time but only one is selected by S1. The outputs are: manually controlled output, triangular wave output (for testing the 'regulator' response) and a square wave output (for testing the 'servo' response).

The manual output is adjusted by RV3a. The low and high limits are governed by RV2 and RV4. These are normally set so that the minimum and maximum voltages correspond to output pulses of 1ms and 2ms. These limits also set the high and low points on the triangular and square waveforms.

The triangular waveform is generated using the CA3080 IC (IC5) to switch a fixed current in and out of a capacitor (C4). The frequency of the waveform generated is a function of the time taken for the voltage on C4 to change from the high limit to the low limit and back again. This is governed by the amplifier bias current, which is set by RV3b. The slowest time is set by RV5. The direction of the output current from IC5 is governed by the 'D' type flip-flop IC2a in a similar manner to the pulse generator. However, IC2a is driven in a different way. Whilst the voltage on C4 is in between the high and low limits the outputs from IC4b and IC4c are low. When the voltage on C4 exceeds the high limit the output on IC4c goes high and resets IC2a. This then makes Q low and $\overline{Q}$ high and C4 starts to discharge. When the voltage on C4 goes below the low limit IC4b sets IC2a and C4 starts to charge. IC4a is purely a buffer amplifier.

The square waveform is generated by a simple add-on to the triangular waveform generator described above. IC6a and IC6b are analogue switches. The analogue inputs are connected to the high and low limits, and the logic inputs (pins 12, 13) are connected to the Q and $\overline{Q}$ outputs of IC2a. Hence while C4 is charging, the output 'C' is connected to the high limit, and while C4 is discharging, the output 'C' is connected to the low limit. See Figure 3 for waveforms.

Construction

This is straightforward. Refer to Figure 4 for the pcb layout and legend. Some care should be taken to avoid static charges when handling the CMOS IC's. Try to fit these last if possible, and always fit them after the power supply smoothing capacitors (C5 and C6) have been installed. Solder the power rail pins first (pins 7 and 14). Otherwise solder at will! A good plan is to do resistors first, then capacitors then the three wire links, using cut off resistor leads, and lastly the IC's. It is not necessary to connect all the 4 outputs. These can be connected in parallel if extra power is needed. When connecting the output sockets make sure that the correct wire goes to each pin. Also take care when testing different servos. There are some manufacturers who use the same sockets but different pin conventions.

Figure 5 shows box cut-out details. Mount the completed board into the box using M3 fixings as shown in Figure 6. Cut the shaft of RV3 to approximately 12mm, and fit a knob. The tang of S1 should also protrude through the slot cut in the side of the box. Fit the lid with the power wires and output connections protruding through the notches. To finish, stick on the front panel.

Set-up and Testing

The Servo Tester was designed to be powered by a 4.8V standard radio control battery pack. Alternatively, a 5V 1A power supply could be used.

Start by positioning all the potentiometers in their mid-positions, and setting the selector switch S1 to manual. Connect the battery/power supply. If an oscilloscope is available, the frame can be set to 20ms by adjusting RV1. This is not critical. Some radio control systems have a variable frame. Here the frame is set by the sum of the pulse widths of all the channels plus the 'sync' pulse, which is usually about 8ms long. Hence on a seven channel system the frame can vary from 15ms to 22ms.

Next set the high and low limits (RV2 and RV4). A good starting point is to adjust these so that the ends of RV3a are at 1.8V and 2.8V. Final setting can then be performed using an oscilloscope or by using a servo on which the output arm movement range has been noted from its use on another radio control system. Adjust RV2 to give 2ms with RV3 fully clockwise and RV4 to give 1ms with RV3 fully anticlockwise. There is some interaction between these settings so it will be necessary to alternately adjust RV2 and RV4 several times.

Now connect a servo (if you have not done so already). Movement of RV3 should give a corresponding movement in the servo. Set S1 to triangular wave. The servo arm should now be moving from one extreme to the other at a rate determined by RV3. With RV3 in the fully anticlockwise position, adjust RV5 to give the slowest desired transit time. A time of about 50 seconds is recommended.

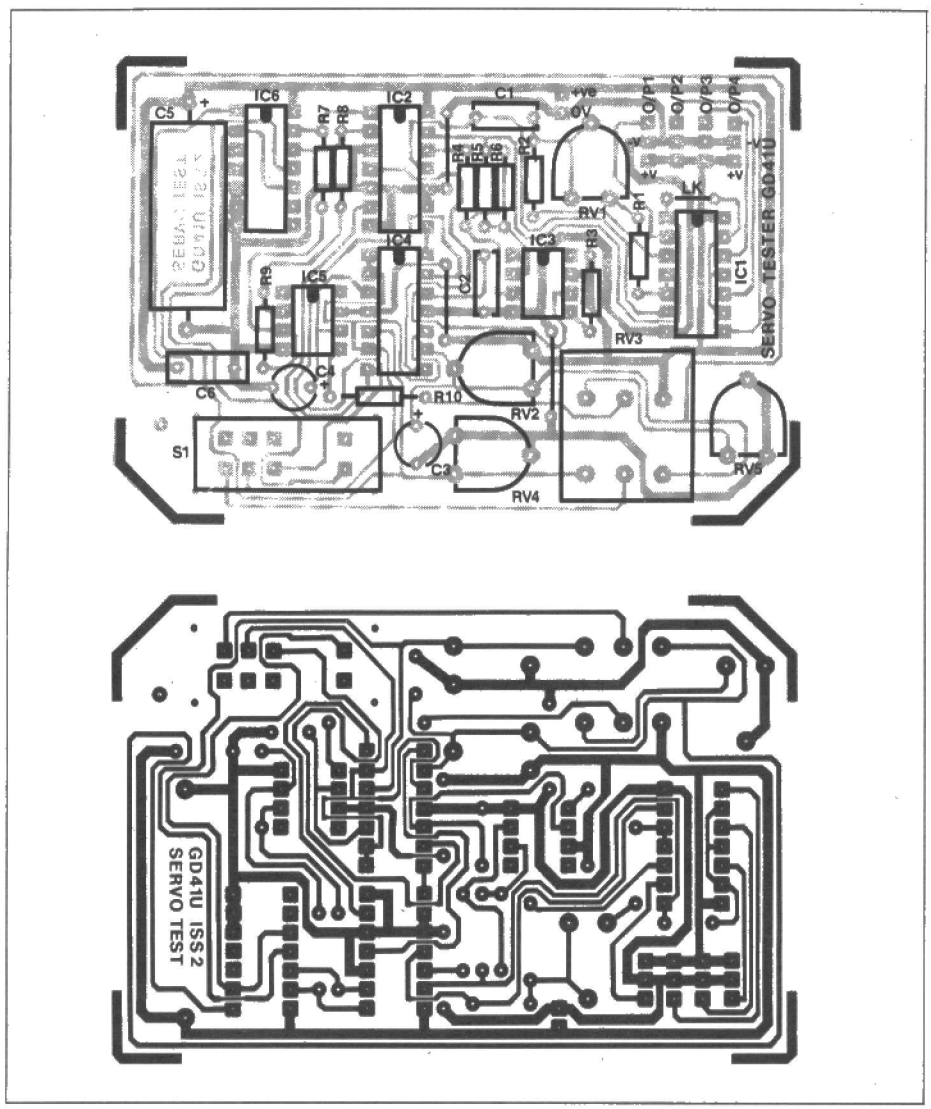


Figure 4. Pcb layout and circuit references.

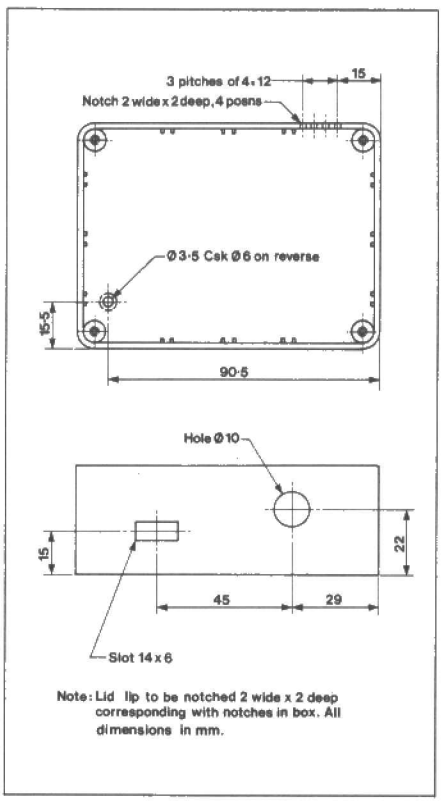


Figure 5. Box drilling.

Use of the Servo Tester

1. Servo Travel

Use the manual control to set the servo from one extreme to the other. Then with a protractor measure the servo travel. Typical values are 70° - 90° for regular servos or 180° for 'retract' servos.

2. Servo Resolution (or Sensitivity)

Set the selector switch (S1) to the mid-position (triangular wave) and set

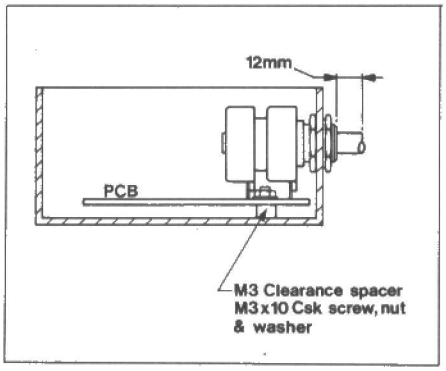


Figure 6. Mounting pcb in box.

RV3 fully anticlockwise. As the pulse slowly changes the servo will respond in small jumps. The servo travel divided by the number of jumps will give the resolution (typically 0.5°). If the slowest transit time has been set to 50 seconds it will only be necessary to count the jumps over 10 seconds and multiply by 5. This test is also useful for showing up any problems with the servo feedback potentiometer.

3. Servo Transit Time

Start with S1 in the squarewave position and RV3 fully anticlockwise. The servo will now switch from one extreme to the other every 50 seconds. Slowly turn RV3 clockwise while listening carefully for the gaps in the servo movements. When these disappear the servo is moving at its maximum speed. Measure the time for 20 swings and divide by 20 to get the transit time, (typically 0.3 to 0.5 seconds). This can be divided by the servo travel to give the servo speed in terms of seconds per degree.

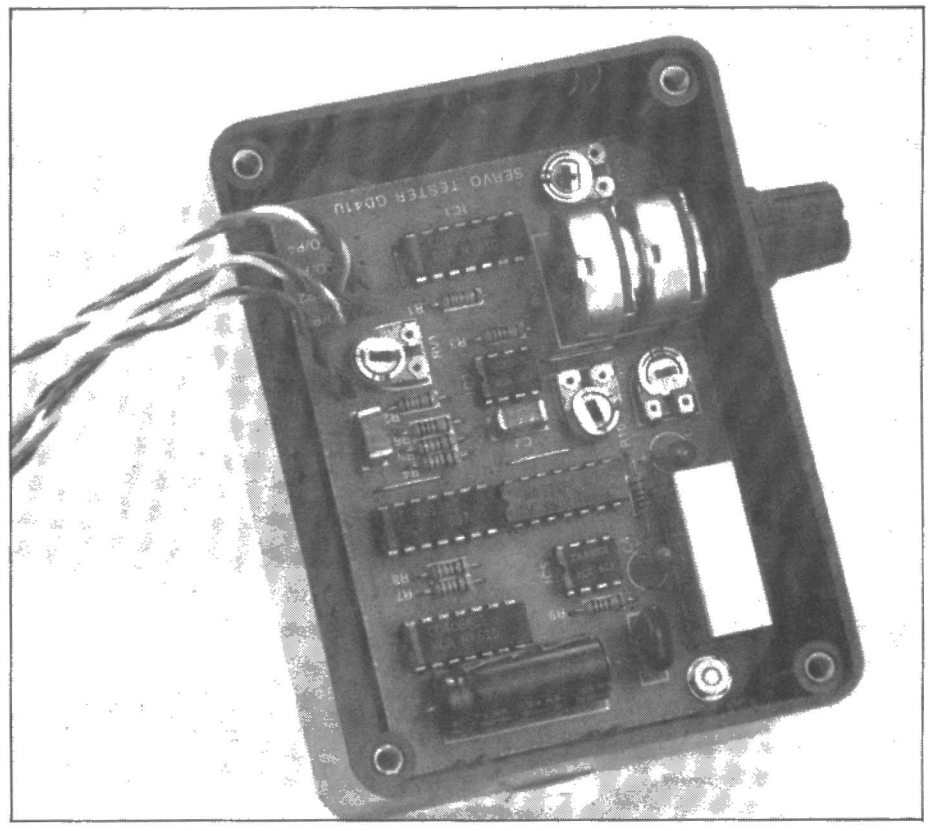
4. Overshoot

With S1 in the squarewave position and RV3 set to get the servo to move full travel about once per second, use a protractor above the servo arm to measure the overshoot, (typical values 0 - 5°).

5. Compare Two Servos

Plug both servos into the tester and run through all the tests. The advantage of doing two at once is that one can get a feel for their differences.

One last thought. Before descending on your local model shop to test his servos, make absolutely certain that your tester is working correctly on each of the outputs, and, of course, that the pin conventions that you have used on your sockets correspond to the pin conventions of the servos being tested.

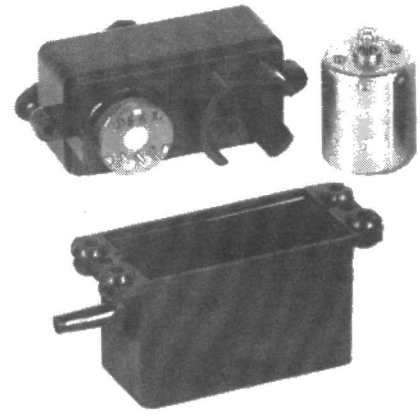


Servo Mechanism

A servo mechanism supplied in kit form is available complete with self contained 5kΩ potentiometer, with end stops on the output shaft. Standard four corner mounting, with four PVC grommets included for insertion into the mounting holes to provide for some insulation against shock and vibration. A PVC cable strain relief is included for wires leaving the servo case. The servo uses the miniature motor YG12N which is retained in position with two screws, and is supplied as part of the mechanism. The servo is provided with a single cross-T output actuating arm. Overall size: 39mm x 39mm x 19mm. Fixing centres: 46 x 11mm x 6BA. Weight: 30 grams with motor.

Order As YG14Q (Servo Mechanism)

Price £8.95



SERVO TESTER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film

R1	56k	1	(M56K)
R2	220k	1	(M220K)
R3	47k	1	(M47K)
R4,5,7,8,10	22k	5	(M22K)
R6,9	10k	2	(M10K)
RV1	47k Sub-min. Hor. Preset	1	(WR60Q)
RV2	22k Sub-min. Hor. Preset	1	(WR59P)
RV3	4k7 Dual pot Lin.	1	(FW94F)
RV4	10k Sub-min. Hor. Preset	1	(WR58N)
RV5	1k Sub-min. Hor. Preset	1	(WR55K)

CAPACITORS

C1	100nF Poly-layer	1	(WW41U)
C2	68nF Poly-layer	1	(WW39N)
C3,4	33μF 10V Tantalum	2	(WW74R)
C5	1000μF 10V Axial Electrolytic	1	(FB81C)
C6	100nF Mylar	1	(WW21X)

SEMICONDUCTORS

IC1	4069UBE	1	(QX25C)
IC2	4013BE	1	(QX07H)
IC3,5	CA3080E	2	(YH58N)
IC4	LM324	1	(UF26D)
IC6	4066BE	1	(QX23A)

MISCELLANEOUS

S1	Switch R/A DT3T	1	(FV02C)
	Servo Tester PCB	1	(GD41U)
	Knob K14A	1	(FK38R)
	Box MB2	1	(LH21X)
	M3 Spacer ¼in.	1 Pkt	(FG32K)
	M3 x 10 Csk. Pozi-screw	1 Pkt	(LR57M)
	M3 Washer	1 Pkt	(BF62S)
	M3 Nut	1 Pkt	(BF58N)
	Hook-up wire Black	1 Pkt	(BL00A)
	Hook-up wire Red	1 Pkt	(BL07H)
	Hook-up wire White	1 Pkt	(BL09K)
	Servo Tester Front Panel	1	(FP75S)

A complete kit of all parts is available for this project:
Order As LM23A (Servo Tester Kit) Price £10.95
The following items in the above kit list are also available separately, but are not shown in the 1987 catalogue:
Servo Tester PCB **Order As GD41U Price £1.98**
Servo Tester Front Panel **Order As FP75S Price £1.20**

WHICH FET?

by J.K. Hearfield

Once upon a time, there were thermionic valves. A valve (for those who have never had to use one) is a large, evacuated glass bulb containing an intricate structure of metal electrodes, and which works on the principle of controlling the flow of an electric current by means of an influencing electric field. In effect, the device is a voltage-controlled resistor.

Thermionic valves grew to become marvellously complex, and the systems they made possible laid the foundations of the modern electronics industry, but they were far from ideal. They were bulky, and inefficient. They had to be 'warmed up' before they would work, to the point where they were too hot to touch. Most important, they were so unreliable (by modern standards at any rate, though it is not unusual for a valve's useful life to be counted in years) that each valve came with its own built-in base plug connector (which of course did not actually improve reliability).

In the late 1940's, a group of researchers at Bell Labs were consequently trying to make a better valve. It was known that semiconductors had some interesting properties, and they were experimenting with germanium. Their idea was to pass a current through a thin film of the material, controlling the current by applying an electric field via a third electrode which was insulated from the semiconductor. It didn't work very well, and was abandoned in favour of other lines of thought which led to the point-contact transistor and eventually to the p-n junction transistor. By the time the concept was tentatively revived a few years later, junction transistors were already firmly established.

But the idea refused to die. Field-effect transistors; transistors whose current was controlled by an electric field rather than by an input current, began to be manufactured in the early 1960's. The first types used the field across a reverse-biased p-n junction, and were therefore known as Junction gate Field-Effect Transistors, or 'JFETs', and sometimes 'JugFETs'. Later it was possible for the metal control electrode to be fully insulated from the semiconductor by a layer of oxide; this process became known as Metal-Oxide-Silicon, or MOS. Their intrinsically high input resistance and good high-frequency performance made FETs a better choice for some applications, though at that time they tended to be unreliable and easily damaged. The technology was gradually perfected though, and eventually it became clear that integrated circuits could be manufactured much more easily if MOS field-effect transistors were used instead of bipolar transistors. It took over thirty years, but the semiconductor version of the valve has made possible systems so complex that they literally could not ever have been built using the early thermionic valves.

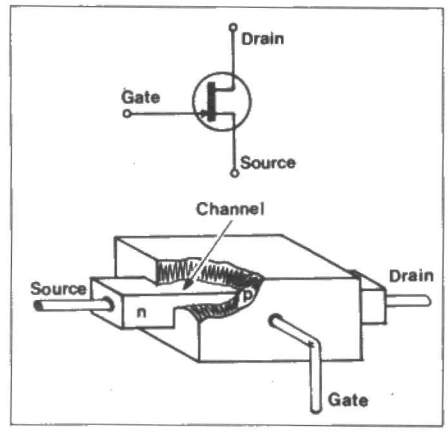


Figure 1. The channel in a JFET is effectively surrounded by the gate.

JFETs

In order to describe how field-effect transistors operate, it is necessary first to explain briefly how the field is applied and what it does.

Depletion Zone

Silicon is called a 'semiconductor' because it doesn't conduct current very well. Current is carried by electrons, of course, and silicon doesn't possess many free electrons. So to improve its conductivity, trace amounts of other materials are added. If the result is a surplus of (negative) free electrons, the resulting material is known as 'n-type', and if instead there are even fewer electrons than there should be normally, giving a surplus of 'holes', it is called 'p-type'. A p-n junction is formed when the semiconductor material changes abruptly from n-type to p-type. Now, some of the free electrons flying around on the n-type side near the junction inevitably find their way across to the p-type side. Once there, they quickly find 'holes' to hide in. The result of this migration is that there are eventually almost no free electrons near the junction in the n-type material and almost no free holes on the p-type side. The region around the junction becomes effectively a 'no-go' area for both electrons and holes, and is consequently known as the depletion zone.

If now a voltage is applied across the junction which makes it easier for the electrons to cross it, more of them will make the one-way journey, and the depletion zone will expand. This happens when the junction is reverse-biased, that is, when the p-type side is

deliberately made more negative than the n-type side, and it is this effect which FETs exploit.

Structure

A JFET consists of a conducting 'channel' through a 'gate', as shown in Figure 1. The n-type channel and p-type gate form a p-n junction which surrounds the channel, and the junction's depletion zone naturally extends into the channel on all sides.

Figure 2 shows the JFET in cross-section. Connections are made to each end of the channel. The 'drain' corresponds to the collector of a bipolar transistor, and the 'source' to the emitter. The drain of an n-channel JFET is normally kept at a more positive potential than its source, so that electrons flow from source to drain. The gate contributes practically nothing to the channel current, so the drain and source currents are the same.

Operation

Suppose, to begin with, that there is only a small voltage difference between drain and source, and that the gate-source voltage is also small. Some current will be flowing down the channel from drain to source. The channel is really just a resistor, so increasing the voltage across it (the drain-source voltage) causes the current to increase proportionally. Current cannot flow through the depletion zone, of course, for (by definition!) in this region there is nothing to carry it. The current is thus restricted to that part of the channel unaffected by the depletion zone, see Figure 3a. But the thickness of the depletion zone depends on the gate-source voltage. If the gate is made more negative, the zone expands, narrowing the channel and squeezing the current more and more into the centre. The channel's cross-sectional area is now smaller, so its effective resistance is greater, so less current flows for a given applied voltage. The JFET under these conditions behaves as a voltage-dependent variable resistor. If the gate-source voltage is made sufficiently negative, the depletion zone extends over the whole channel, and no current at all can flow. The JFET is then said to be in a 'pinch-off' condition.

The voltage controlling the width of the depletion layer is applied between the gate and source. But the drain is more positive than the source, so there is a greater reverse bias across the p-n junction at the drain end of the channel than at the source end. It follows that the depletion zone is wider at the drain end, and that its width here depends at least as much on the drain-source voltage as on the gate-source voltage. As the drain-source voltage is increased, the depletion zone bulges inward towards the centre of the channel until pinch-off occurs, see Figure 3b. Electrons can still drift through the pinched-off region

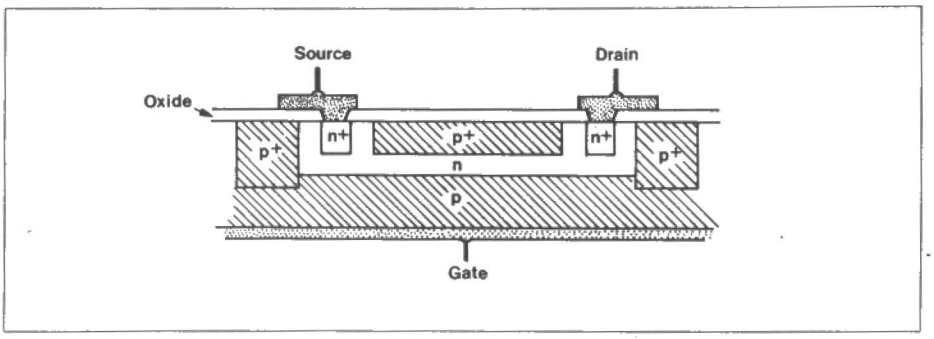


Figure 2. N channel JFET structure.

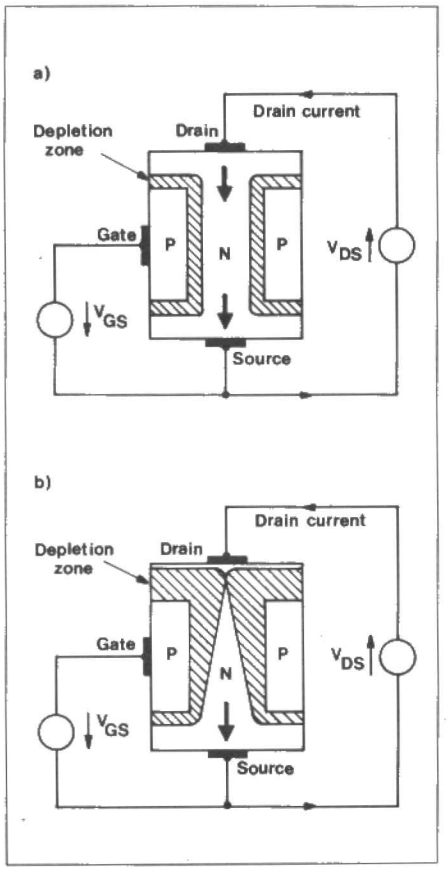


Figure 3. The depletion zone width depends on V_{GS} and V_{DS}. (a) The depletion zone is small when V_{GS} and V_{DS} are small. (b) The channel is pinched off when V_{DS} is large enough, but drain current still flows.

however, so channel current continues to flow, but the current does become (almost) independent of the drain-source voltage.

The output characteristics of a typical JFET are shown in Figure 4. At low values of V_{DS} (Drain-Source Voltage) each characteristic is a straight line whose slope depends on V_{GS} (the Gate-Source Voltage). When V_{DS} is greater than about 2V, I_D is almost constant for a given V_{GS} and independent of V_{DS}. I_D becomes larger as V_{GS} is made more positive.

Transfer Characteristic

The transfer characteristic (I_D against V_{GS}) can be inferred from the output characteristics, and is shown in Figure 5. It is clearly far from linear, especially when V_{GS} is close to pinch-off. In fact, it is an almost perfect square-law function. This limits the usefulness of the JFET as an amplifier, since it can only handle small signals without distortion becoming too much of a problem, but makes it a good RF amplifier or mixer.

The device gain is the slope of the transfer characteristic, that is, the ratio of the output change (in drain current) resulting from an input change (in gate-source voltage). Current divided by voltage is an admittance, Y, (the reciprocal of impedance, Z) and has the units of 1/ohms, or Siemens (S). JFET manufacturers usually specify gain as Y_{fs}, the FET's forward transfer admittance. A typical Y_{fs} of 5 mS means that an output current swing of 0.1mA would require an input voltage swing of (0.0001/0.005) volts, or 20mV.

Measurement of Pinch-off Voltage & Zero-bias Drain Current

Though apparently identical devices will probably have much the same gains, their pinch-off voltages may be wildly

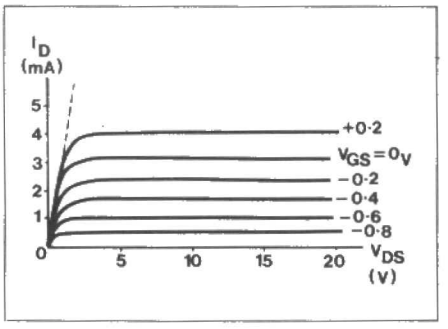


Figure 4. Output characteristics (N channel JFET).

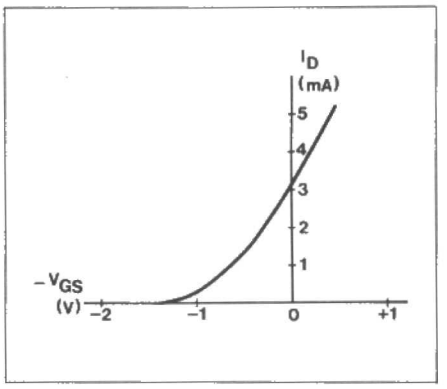


Figure 5. Transfer characteristic (N channel JFET).

different. Figure 6 illustrates the possible values the pinch-off voltage (V_P) and zero-bias drain current (I_{DSS}) can take for a 2N3819. It is sometimes useful to be able to measure these parameters quickly, and Figure 7 shows how this can be achieved using just a multimeter and a voltage source. The measurement of I_{DSS} is self-evident, V_{GS} must be zero if the gate and source are connected together. To measure V_P the meter is switched to a voltage range, so that it behaves as a very high resistance. A minute drain current flows, as the JFET is almost (but not quite) in pinch-off, and the meter reads the gate-source voltage at which this occurs.

Absolute Maximum Ratings

JFET manufacturers warn users against overstressing the p-n junction by specifying limits for the highest tolerable forward current and reverse bias. Since the device is almost never operated with the junction forward-biased, the most important practical limitation is that the gate-source voltage must not be too large. The maximum allowable voltage is specified on the data sheet as, for example, $V_{(BR)GSS}$ or V_{GSO} or BV_{DGO} and is typically 30 volts or so. It is perhaps less obvious that a similar limit applies to the drain-source voltage. Yet since the gate is often at almost the same potential as the source, the drain-source voltage is close to the drain-gate voltage. The reverse bias across the junction is highest at the drain end of the channel, so the junction will break down here if the reverse bias becomes too great.

Manufacturers also specify the maximum power dissipation and channel current their devices are designed to withstand, and it is sensible not to exceed them.

Temperature Effects

As the temperature goes up, so does the leakage current of a p-n junction. The leakage current in this case is of course the JFET's gate current, and it can be expected to increase by a factor of 10 for every 40° rise in temperature.

P-channel JFETs

There is no reason why the channel cannot be made of p-type material instead of n-type, and many such devices exist. They must be biased such that the source is more positive than the drain, and the gate is more positive than the source, exactly the opposite conditions to those needed by an n-channel device, but otherwise their behaviour is very similar to that of n-channel JFETs.

Models

A simple low-frequency model for a JFET is shown in Figure 8a. Indeed, since it consists of just one component, a current generator, it couldn't really be much simpler. The model assumes that the device is operating in pinch-off,

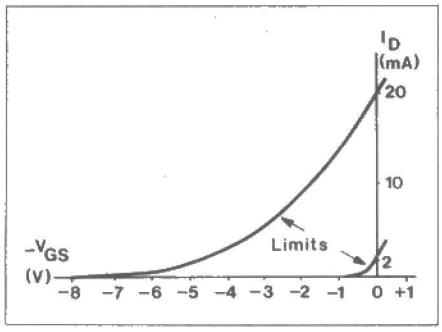


Figure 6. A JFET's transfer characteristic is often not tightly defined, I_{DSS} for a 2N3819 may be anywhere between 2 and 20mA.

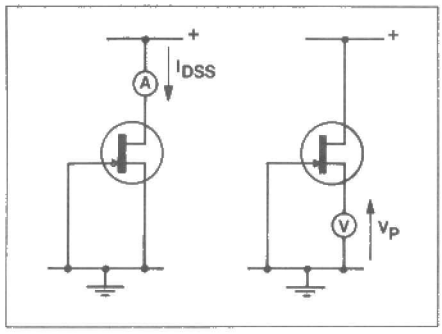


Figure 7. Measuring I_{DSS} and V_P.

where the drain current depends almost solely on the gate-source voltage. In effect, it assumes that the output resistance is negligibly high compared to the load. The 'gain' g_m is the slope of the transfer characteristic (I_D against V_{GS}) at the operating point. More precisely, it is the resistive part of the forward transfer admittance (Y_{fs}), but since this model applies only at low frequencies, there is no great harm in ignoring the effects of internal capacitive feedback.

Using the model is easy. The first step is to establish g_m by choosing the drain current at which the device will operate. The higher the current, the higher g_m will be. Then choose a load, R_L. All the generator current flows through the load, so the stage voltage gain is just:

$$A = g_m R_L$$

High-frequency Behaviour

Designing JFET circuits that work well at high frequencies is a difficult and demanding task, and one quite outside

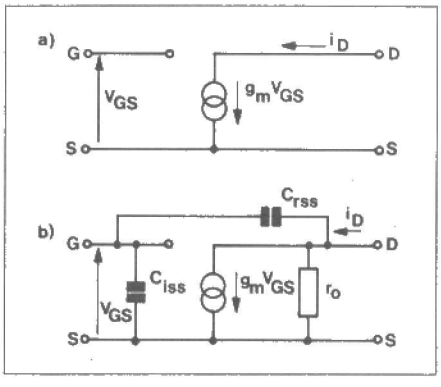


Figure 8. JFET models, (a) Low frequency, (b) High frequency.

the scope of this article. JFETs (and MOSFETs) are used extensively in receiver front-ends, as their inherent low noise, large gain-bandwidth product and low cross-modulation and inter-modulation distortion performance make them superior to bipolar junction transistors. Comparing the high-frequency model of Figure 8b with its low-frequency counterpart, the main differences lie in the inclusion of input and feedback capacitors. The input capacitance (C_{is} or C_{iss}) is typically 4pF, whilst the feedback capacitor (C_{rs} or C_{rss}) may well be rather less than 1pF.

Choosing a JFET

The Maplin catalogue lists seven JFETs, all of them n-channel. In ascending order of price, they are:

2N5459, BF244, MPF102, 2N5458, 2N3819, 2N4393, BFW10.

Different applications demand different strengths. The BFW10, for example, is designed for use in wide-band amplifiers, though it has low noise too at audio frequencies. The BF244 also has low noise, but is intended for use in audio amplifiers. The 2N4393 by contrast is optimised for use as a switch, able to dissipate substantial amounts of power and with an 'on' resistance of less than 100 ohms. Of the general-purpose types, the 2N5458/9 have very low input currents.

MOSFETs

JFETs separate the gate from the channel by means of a reverse-biased p-n junction. MOSFETs use a thin layer of insulating material instead, usually silicon dioxide. As a result, the input (gate) current of a MOSFET is much lower even than that of a JFET.

The properties of an MOS transistor depend more on its geometry than on its actual size, so devices have been steadily getting smaller as the technology has advanced. This in turn has meant that more and more of them can be accommodated on a single integrated circuit, and the results of this revolution are all around us.

Operation

Like JFETs, MOSFETs work on the principle of controlling the device current by varying the depth of a depletion zone inside a conducting channel. But unlike JFETs, the depletion zone in MOSFETs is created by applying an electric field across the channel between the gate and the substrate. Figure 9 shows the structure of an n-channel device. When the gate is made more negative than the substrate, the electric field pushes electrons away from the gate and so creates a depletion zone extending downwards from the gate oxide layer into the channel. The effective depth of the channel thus depends on the gate voltage, just like a JFET.

This type of device is known as a Depletion-Mode MOSFET, because the action of the gate voltage is to deplete the channel of current carriers. But consider for a moment what would happen if the gate were made more positive than the substrate. Extra electrons would be attracted towards the gate, and the channel would effectively become even deeper. It is quite possible to operate a Depletion-Mode MOSFET like this (though not a JFET) as the characteristics of Figure 10 illustrate.

Taking the argument to its logical conclusion, what would happen to a device with no built-in channel when its gate is made more positive than its substrate? The answer is that when the potential difference becomes sufficiently large, a channel magically springs into being out of nowhere and the current flow along it depends once again on the gate-source voltage. This type of device is known as an Enhancement-Mode MOSFET, and its structure and characteristics are shown in Figures 11 and 12. Enhancement-Mode MOSFETs are in fact very commonly used in integrated circuits. For example, CMOS circuits are built from a combination of n-channel and p-channel enhancement-mode devices.

Characteristics

The characteristics of a MOSFET are, not surprisingly, quite similar to those of a JFET. Suppose the drain-source and gate-source voltages are both small. The gate-source voltage controls the depth of the depletion zone, the greater the voltage, the wider the depletion zone and the higher the effective resistance of the channel. Now suppose the drain-source voltage is increased. The depletion zone gets wider at the drain end of the channel and eventually the channel is pinched off. After this, the channel current (I_D) remains almost constant.

The models of Figure 8 apply also to MOSFETs.

Temperature Effects

Unlike bipolar transistors, a rise in temperature causes the device current to fall. This means that thermal runaway cannot happen, and allows MOSFETs to be connected in parallel without the need for current-sharing resistors.

Electrostatic Damage

Static charge can accumulate on the gate because the gate leakage current is so small. If the resulting potential difference between gate and source becomes sufficiently large, it will punch a hole straight through the insulating oxide layer and the device will in consequence be permanently damaged or destroyed. Manufacturers do their best to prevent this by building in clamp diodes and shipping the parts with all their pins held at the same potential, either by being inserted in conductive foam or bound in a common wire ring. Nevertheless, it is still embarrassingly easy to accidentally destroy an MOS device, just walking across a nylon carpet and touching it can be enough.

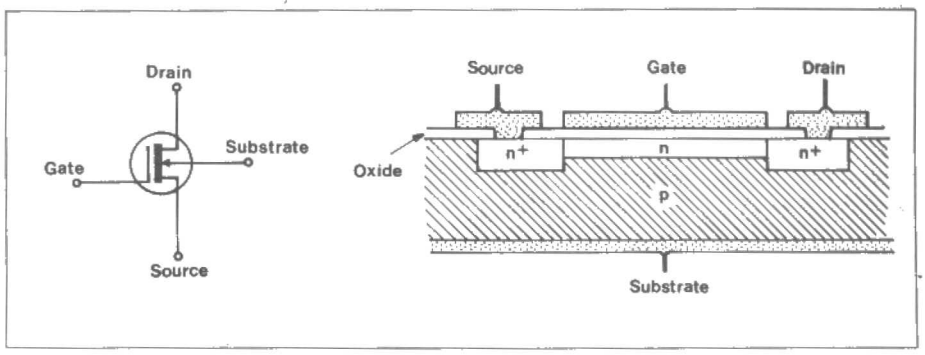


Figure 9. N channel depletion-mode MOSFET structure.

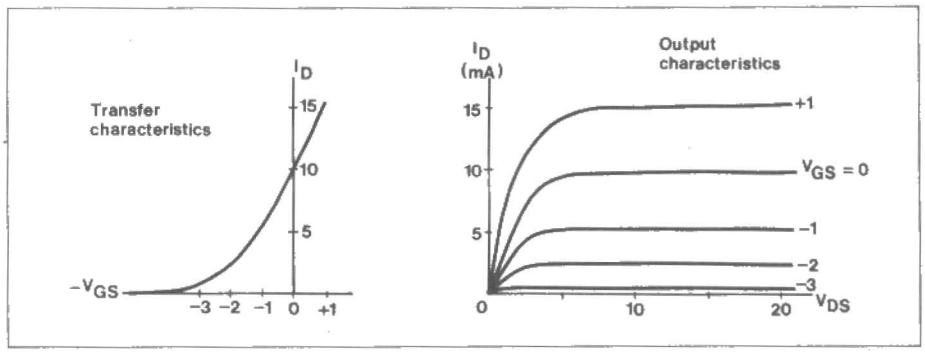


Figure 10. N channel depletion-mode MOSFET transfer and output characteristics.

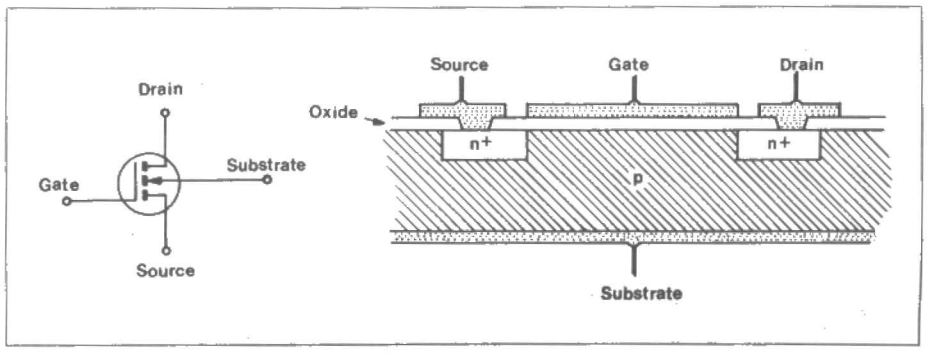


Figure 11. N channel enhancement-mode MOSFET.

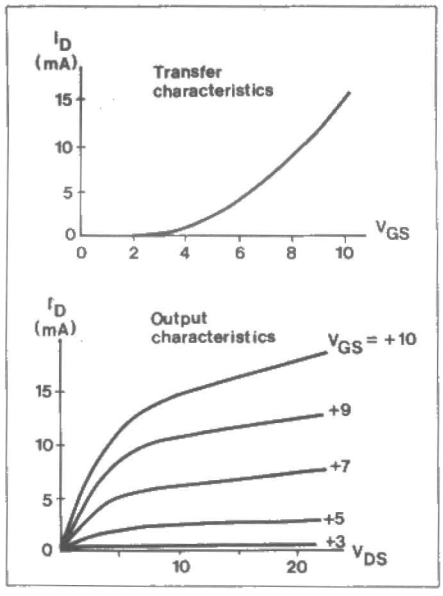


Figure 12. N channel enhancement-mode MOSFET transfer and output characteristics.

Choosing a MOSFET

A common application for MOS small-signal transistors is as RF amplifiers or mixers. Their low noise and excellent high frequency performance make them ideal as front-end amplifiers. Such devices often have two independent gates, G1 and G2. The incoming signal is applied to G1, whilst the voltage applied to G2 is derived from the receiver's Automatic Gain Control line and is used to modulate the G1 transfer characteristic. Four such devices are listed in the Maplin catalogue. In ascending order of price, they are:

3SK88, 40673, 3SK124, 3N140.

Each offers a slightly different price/performance trade-off.

If your problem is switching a high current efficiently, the 2N7000 'Fetlington' may be the answer. It can switch over 100mA with an 'on' resistance of less than 5 ohms given an input voltage swing of 5 volts.

VMOS Power Devices

It is perhaps surprising that one of the most important application areas for

MOS transistors is as power switches. VMOS FETs do however combine the advantages of bipolar power transistors (the ability to handle large currents and high voltages) with those of MOS transistors (high gain and freedom from thermal runaway) and as a result they are rapidly becoming the preferred choice. The structure of a typical device is illustrated in Figure 13.

Current flows vertically through the transistor from source to drain, instead of horizontally just below the gate as in other MOSFETs, through short channels created on each side of the V-grove. This novel approach has led to devices that outperform many conventional power transistors and at the same time simplify system design by interfacing directly to TTL and CMOS logic circuits. Since a VMOS FET (like any other FET) draws practically no gate current, the device driving it need only provide a relatively small voltage swing. But it should be remembered that the FET does have an input capacitance of perhaps 500pF or more which must be charged and discharged quickly by the driver if the FET is to switch at high speed. With proper driver design, a VMOS FET can switch several amps on and off in a few nanoseconds.

Figure 13 shows that the source contacts overlap both the n+ and p

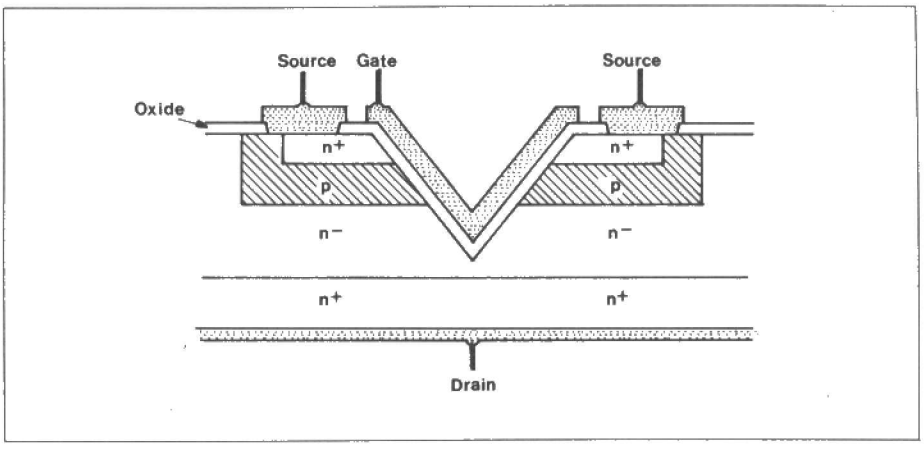


Figure 13. Structure of a VMOS FET.

areas. In consequence, VMOS FETs all have a parasitic diode between drain and source. This doesn't usually cause problems, since the drain is normally held positively of the source, but it can be useful in some applications (switching inductive loads, for example) to have a built-in snubber diode. Some devices also possess an internal protective zener diode connected between gate and source.

Choosing a VMOS Power Fet

If you are looking for a device to control power, you presumably already know how much current it has to handle, the maximum voltage it must withstand, and its worst-case power dissipation. The only real remaining trade-off is between the transistor's 'on' resistance ($R_{DS(ON)}$) and its cost. High-current devices cost more, but have a lower $R_{DS(ON)}$ (and usually a higher C_{iss}). The devices in the Maplin catalogue, arranged in ascending order of price are:

VN10KM, VN46AF, VN66AF,

and

2SJ48 & 2SK133, 2SJ49 & 2SK134, 2SJ50 & 2SK135.

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Weather Satellite Down Converter

by Robert Kirsch Part 2

This is the second article describing a Down Converter for use with the MAPSAT VHF Receiver and Decoder. The previous article covered the Meteosat System with a technical description of the Down Converter and Pre-amplifier, as well as the requirements necessary for the sighting of the aerial system. This article describes the installation and testing of the complete system and also the circuit description and construction details for the Channel Switching Unit.

Aerial and Pre-amplifier

The aerial kit (LM22Y) is supplied with all metalwork pre-drilled and cut to length, all necessary screws, nuts and washers are also included together with full assembly instructions. The ready-built and pre-aligned Pre-amplifier is also included with this kit. **Note:** This kit does not include a mast or lashings, and something suitable should be chosen for your particular installation, bearing in mind the sighting requirements described in the previous article. The system should, if possible, be tested at ground level before the aerial is installed in its final position, see 'Pre-Installation Tests' below.

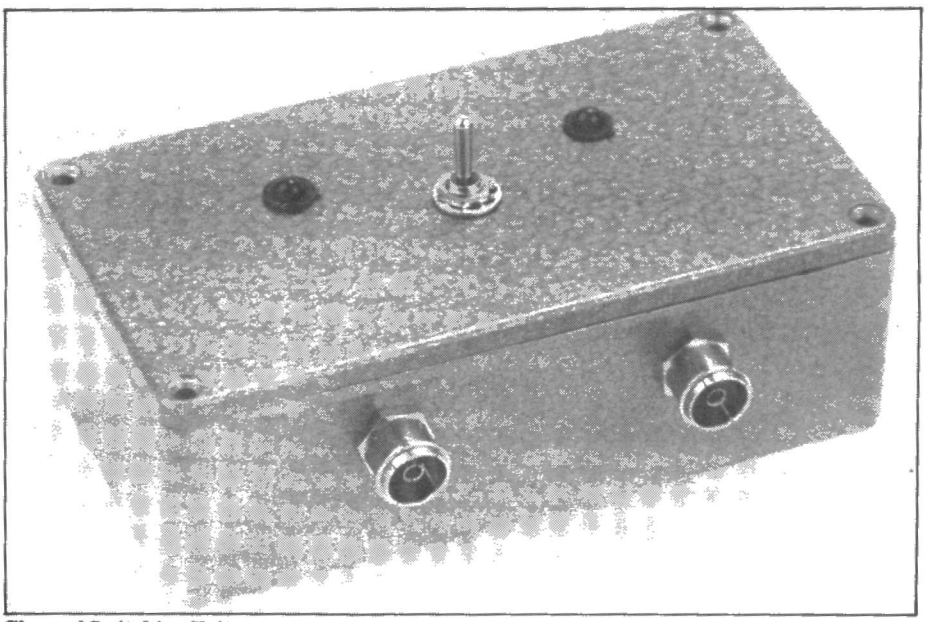
Down Converter

This unit is ready-built and aligned and requires no action at this stage other than roughly determining its final position in order to find the approximate length of feeder that will be used, as this is required during testing.

Channel Switching Unit

This unit is required in order to change the channel being received by the Down Converter. The unit is connected in series with the aerial cable that exits from *the Down Converter, and then* connects to the aerial socket of the Mapsat Receiver.

When the Receiver and Down Converter *are first powered up, channel* 1 is automatically selected. Channel 2 is selected by operating the toggle switch



Channel Switching Unit.

located on the front panel of the control unit in the appropriate direction. This causes a short break in the power supply which is detected by the channel switching logic in the Down Converter, and switches the channel 2 crystal into circuit. The toggle switch, when moved to the channel 1 position, causes a longer break in the supply to the Down Converter and the switching logic will now select the channel 1 crystal.

Circuit Description

Figure 1 shows the circuit of the Channel Switching Unit. Figure 5 of the Down Converter article includes the channel switching logic and crystal oscillator circuits.

The radio frequency signals from the Down Converter enter the unit via SK1 and are directly coupled to the Receiver via C6 and SK2. The supply from the Receiver *(positive on the coax centre conductor* and negative on the screen) is separated from the RF signals by L2 which provides a high impedance to the signals at 137.5MHz, but *has a low* resistance to DC. This supply is connected via the contacts of RL1, L1 and SK1 to the Down Converter.

When the toggle switch is moved to channel 2 position, the input of the inverter IC1e is pulled high, the output goes low and the pulse caused by C8 charging is inverted by IC1f, turns on TR3 and operates RL1 for a short period. The contacts of RL1 are normally made and thus this pulse causes a short break in the supply to the Down Converter. When the switch is moved to the channel 1 position the same sequence of events occur but in this case the pulse length is determined by C7, this being a higher capacity, the pulse is longer and the supply is interrupted for a greater period of time.

The circuit formed by IC1a, b and c is used to mimic the channel switching logic in the Down Converter in order to drive the LEDs that show which channel has been selected. The input to this circuit is via D1 and C3, which are connected to the switched side of the *unit. When a short duration interruption* occurs C3 produces a short positive going pulse at the point when the power is restored, this causes the latch formed *by IC1a* and c to change state. During this process, C1 has remained charged and the output of the inverter IC1b remains low and has no effect on the latch. When

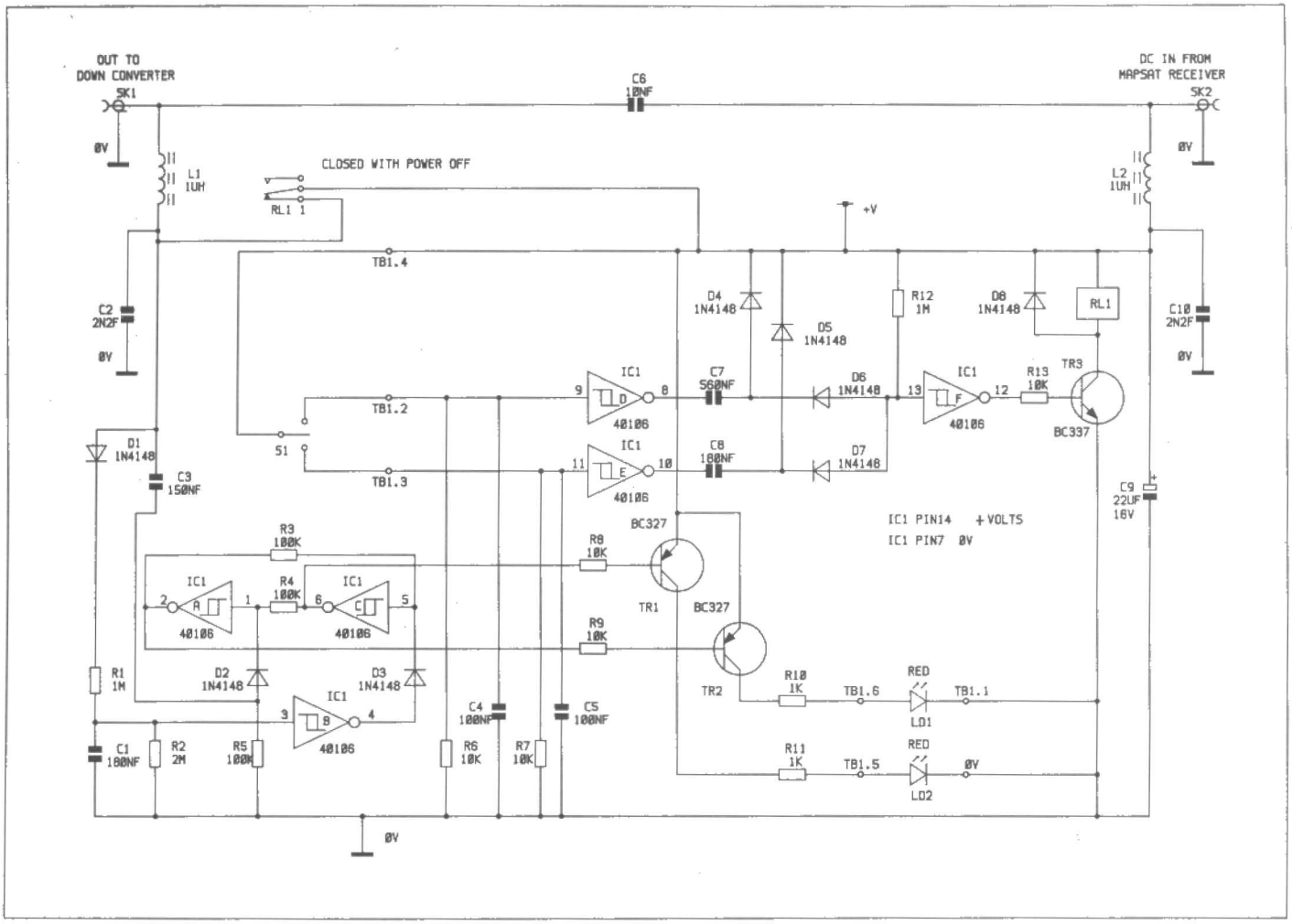


Figure 1. Channel Switching unit circuit.

the longer duration channel 1 pulse occurs (generated at initial switch on), the same sequence occurs but this time C1 has discharged. The pulse from C3 still tries to switch the latch it has held in the opposite state by the output of IC1a being high due to the slow charging time of C1 via R1. The two indicator LEDs are driven by TR1 and TR2 from the appropriate latch outputs.

The channel switching logic in the Down Converter works in the same way, but in this case as the whole power supply is interrupted, it is necessary to maintain the power to IC2 (Part 1, Figure 5) during the switching period. This is accomplished by C18 which is charged via D4. The short duration pulse is produced by C19, and C17 determines the long charge time. In this case the output from the latch is used to bias either D6 and D8 or D9 and D7 on, thus grounding either XT1 or XT2 in the crystal oscillator circuit.

Construction

Referring to the Parts List and the circuit board layout shown in Figure 2, insert and solder all components. **Note:** The two chokes, L1 and L2, are only soldered to the board at *one end* as the other ends connect to the *centre terminal* of the input and output sockets. C6 is not mounted on the circuit board, but is connected directly between the centre

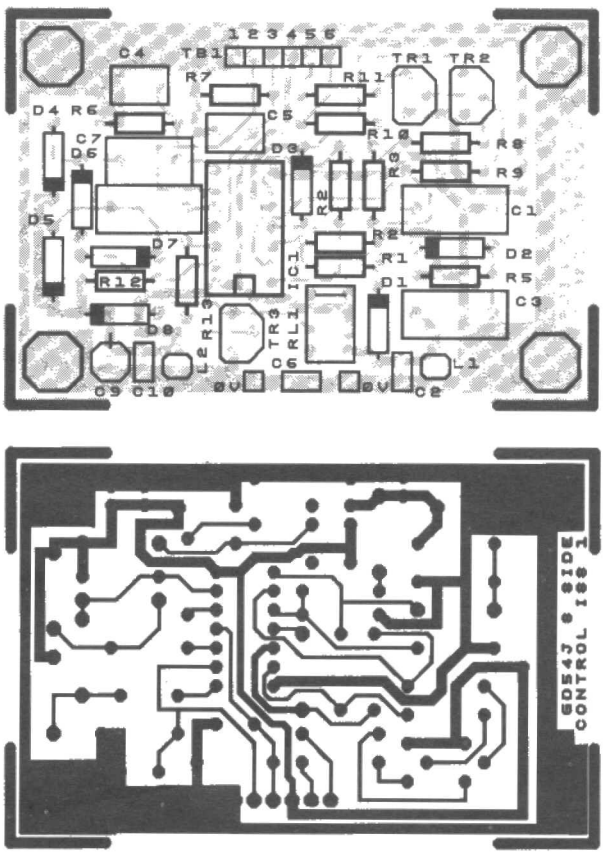


Figure 2. Channel Switching board track and layout.

terminals of the sockets. Drill the die-cast box as shown in Figure 3, and fit the stick-on front panel. Mount the two LEDs and the toggle switch to the lid of the box and terminate about 10cm of ribbon cable to them whilst following the wiring diagram in Figure 4. Terminate the other end of the ribbon cable in the IDC connector, ensuring that the wires are in the correct order. Each wire should be carefully laid in its groove and then firmly pressed into position using an IDC insertion tool.

Fit the two coax sockets to the box with the solder tags on the inside using the screws, spacers, lock washers and nuts provided, and terminate L1 and L2 to the centre pins of the sockets. Connect a short length of tinned copper wire to each of the Veropins on the lower edge of the board, and solder the other end of these to the solder tags on the sockets. The IDC connector may now be plugged onto the circuit board and the lid secured with the four countersunk screws provided. The control unit is now ready for testing.

Modifications to the MAPSAT Receiver

The Mapsat Receiver requires a minor modification in order to supply the extra power required of it by the Down Converter and Pre-amplifier. Remove the top cover from the Receiver to gain access to the circuit board. Locate the resistor R1 near the aerial input coil, and carefully solder a short length of tinned copper wire across this resistor, being careful *not* to make contact with the earth plane surrounding the resistor pads!

Pre-Installation Tests

For these tests the assembled aerial should be attached to a temporary mast in a position that will enable adjustments to be carried out on the pre-amplifier. The aerial should be pointed at un-obstructed sky in the direction of the satellite, see previous article. Connect the F type plug on the end of the cable attached to the Pre-amplifier to the appropriate socket on the Down Converter (SK1). After determining the approximate length of the down lead, prepare this length of cable with coax plugs at each end. Connect this lead to the remaining socket on the Down converter and to the right-hand socket of the Channel Switching Unit. Make up the short coax lead that connects the Channel Switching Unit to the MAPSAT Receiver, using two coax plugs (shown as optional in the Channel Switching Unit parts list). Connect the Receiver to the left-hand socket of the Switching Unit. The MAPSAT Receiver may be powered from batteries for these tests, if it is more convenient than using a mains operated power supply. For these tests the Receiver should be located near the aerial system so that the effect of adjustments can be observed.

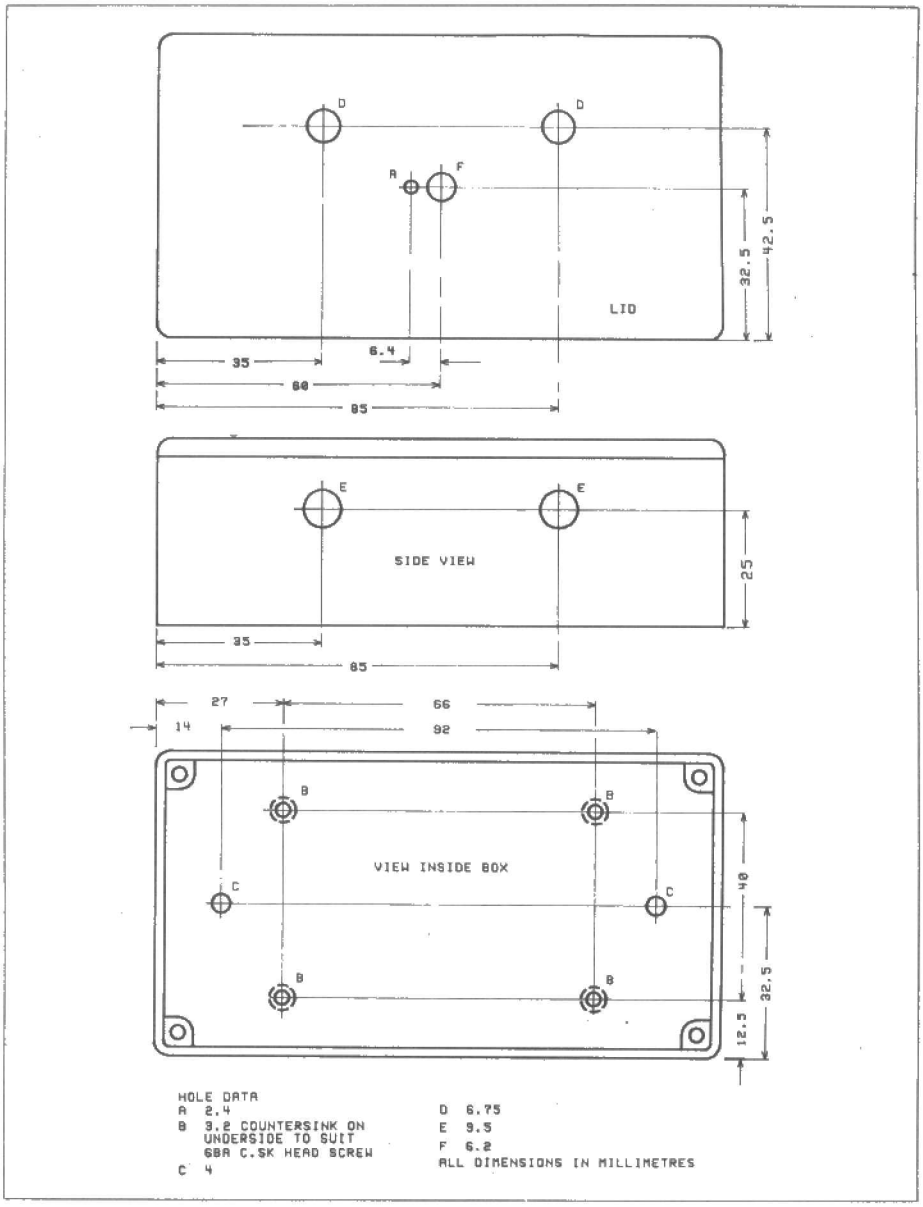
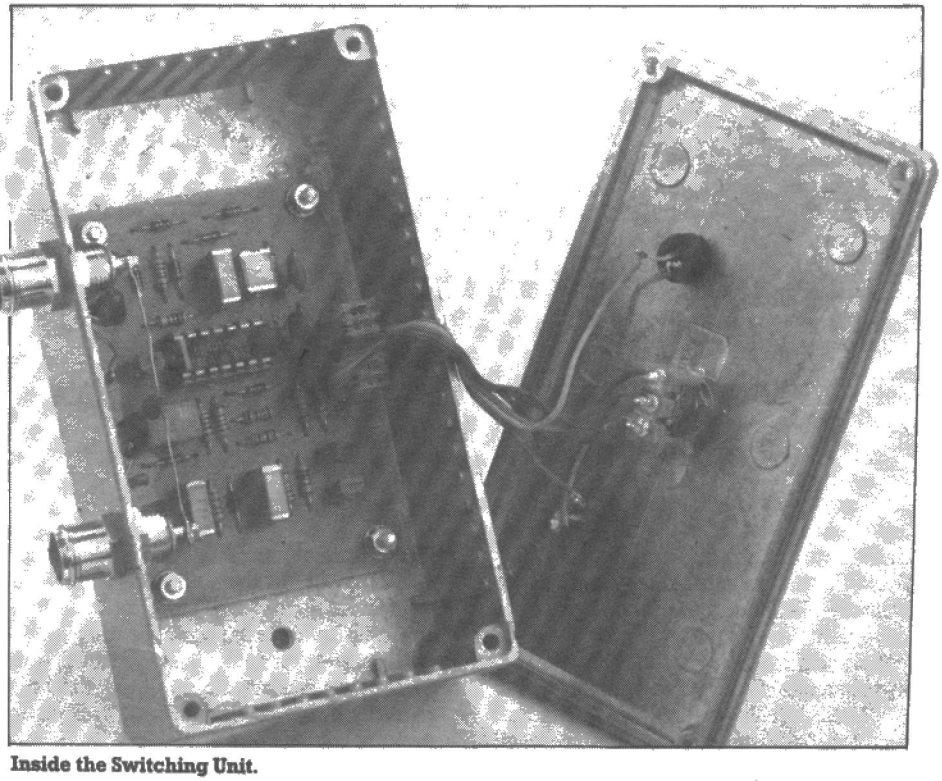


Figure 3. Case drilling.



Inside the Switching Unit.

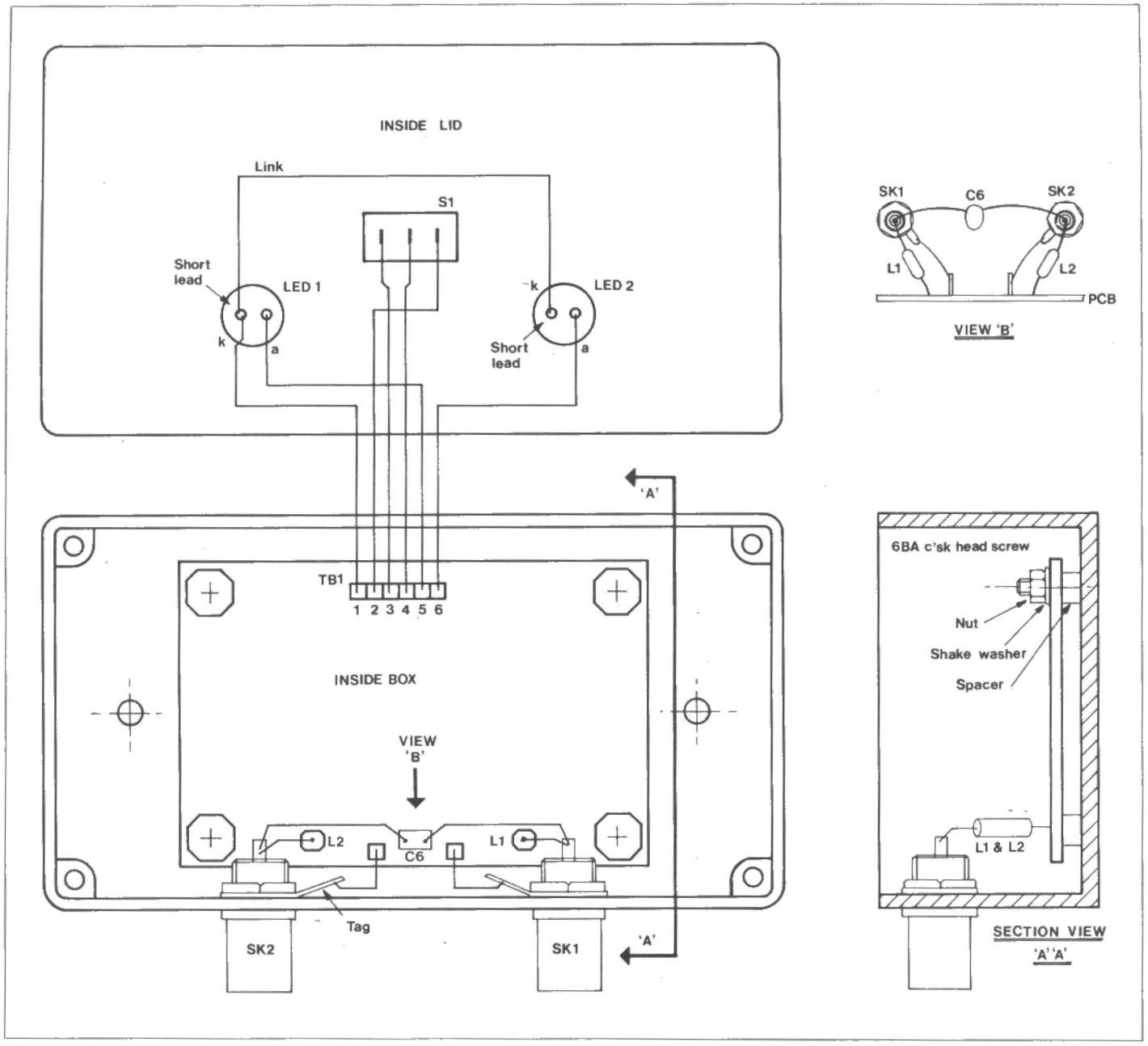


Figure 4. Wiring and assembly.

Switch on the power to the Receiver and check that the channel 1 LED on the Switching Unit is illuminated. Move the toggle switch to the channel 2 position and check that the channel 2 LED is now illuminated, and that the channel 1 LED goes out. **Note:** The toggle switch is centre-biased and must be held in the required position for a short time until the switching sequence is complete. (No more than 2 seconds.) Repeat the test in the opposite direction and check that the LED's return to their starting condition.

Signals are transmitted by Meteosat 2 on channel 1 most of the time, but, it is advisable to check the Prediction Chart (Table 1) to ensure that signals are available. Set the volume control to a convenient level and tune the receiver until signals from the satellite are heard. (Approximately 5 on the tuning dial; 137.5MHz). The position of the aerial should be adjusted for maximum signal strength. *Very carefully* adjust the screw type trimmer on the Pre-amplifier for maximum signal strength. This trimmer is located towards the front of the Pre-amplifier and is accessible through a small hole in the case. After this adjustment has been completed, the hole should be sealed with silicon rubber to prevent the ingress of water.

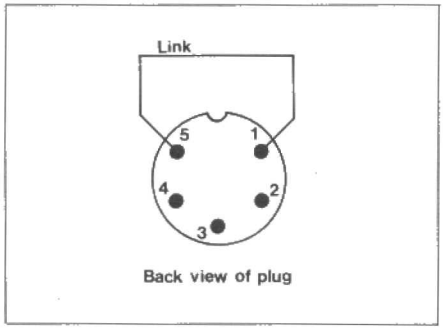


Figure 5. Receiver by-pass plug.

Assuming that a reasonably strong noise free signal is obtained, the unit is now ready for installation in its permanent position.

Using the System

Signals from orbiting weather satellites are usually recorded before being decoded and displayed, as they are only receivable for short periods during the day. The majority of pictures transmitted by Meteosat 2 on channel 1 are updated every hour, so it is often unnecessary to record them, as they may be displayed as they are received. To operate the MAPSAT system without a tape recorder connected, a by-pass plug must be inserted in the socket at the rear of the Receiver in place of the recorder, see Figure 5. The audio level out of the Receiver may be found to be too low to operate the Decoder in this mode; if this is the case, resistor R57 on the Receiver board may be reduced in value or shorted out altogether. All pictures

METEOSAT DISSEMINATION SCHEDULE

Hrs Mins	00 UT CH1	00 UT CH2	03 UT CH1	03 UT CH2	06 UT CH1	06 UT CH2	09 UT CH1	09 UT CH2	12 UT CH1	12 UT CH2	15 UT CH1	15 UT CH2	18 UT CH1	18 UT CH2	21 UT CH1	21 UT CH2	Hrs Mins
2	E3 47				E3 11	WEFA 2			E3 22	— —		WEFA 4	E3 34				2
6						— —				— —		— —					6
10	D2 48	BIW 48	D2 6	BIW 6	D2 12	BIVW 12	B2 18	BIVW 18	D2 24	BIVW 24	D2 30	BIVW 30	D2 36	BIVW 36	D2 42	BIW 42	10
14	D1 48		D1 6		C02 12	DTOT 12	C02 18		C02 24	DTOT 24	C02 30		D1 36	DTOT 36	D1 42		14
18	D3 48	AI 48	D3 6	AI 6	C03 12	AIVH 12	C03 18	AIVH 18	C03 24	AIVH 24	C03 30	AIVH 30	D3 36	AI 36	D3 42	AI 42	18
22	D4 48	— —	D4 6	— —	D1 12	— —	D1 18	— —	D1 24	— —	D1 30	— —	D4 36	— —	D4 42	— —	22
26	D5 48	LY 48	D5 6	DTOT 6	D3 12	— —	D3 18	— —	D3 24	— —	D3 30	— —	D5 36	LY 36	D5 42	DTOT 42	26
30	D6 48	LR 48	D6 6		D4 12	LY 12	D4 18	DTOT 18	D4 24	LY 24	D4 30	DTOT 30	D6 36	LR 36	D6 42		30
34	D7 48	DTOT 48	D7 6		D5 12	LR 12	D5 18	CTOT 18	D5 24	LR 24	D5 30	ETOT 30	D7 36	WEFA 5	D7 42		34
38	D8 48		D8 6		D6 12	ETOT 12	D6 18	ETOT 18	D6 24	CTOT 24	D6 30		D8 36	— —	D8 42		38
42	D2 1	BIW 1	D2 7	BIW 7	D2 13	BIV 13	D2 19	BIV 19	D2 25	BIV 25	D2 31	BIV 31	D2 37	BIVW 37	D2 43	BIW 43	42
46	D9 1	LX 48	D9 7		C02 13	LX 12	C02 19		C02 25	LX 24	C02 31		D9 37	LX 36	D9 43		46
50	D1 1	— —	D1 7	AI 7	C03 13	— —	C03 19		C03 25	— —	C03 31		D1 37	— —	D1 43	AI 43	50
54	D3 1	AI 1	D3 7	— —	C3D 13	AI 13	C1D 19	AI 19	C1D 25	AI 25	C1D 31	AI 31	D3 37	AI 37	D3 43	— —	54
58		— —			C2D 13	— —	C2D 19	— —	C2D 25	— —	C2D 31	— —		— —			58

Hrs Mins	01 UT CH1	01 UT CH2	04 UT CH1	04 UT CH2	07 UT CH1	07 UT CH2	10 UT CH1	10 UT CH2	13 UT CH1	13 UT CH2	16 UT CH1	16 UT CH2	19 UT CH1	19 UT CH2	22 UT CH1	22 UT CH2	Hrs Mins
2							C3D 19		C3D 25	ETOT 24	C3D 31						2
6							C4D 19		C4D 25	L2 24	C4D 31						6
10	D2 2	BIW 2	D2 8	BIW 8	D2 14	BIVW 14	D2 20	BIVW 20	D2 26	BIVW 26	D2 32	BIVW 32	D2 38	BIVW 38	D2 44	BIW 44	10
14	D1 2		D1 8		C02 14		C02 20		C02 26	DTOT 26	C02 32		D1 38		D1 44		14
18	D3 2	AI 2	D3 8	AI 8	C03 14	AIVH 14	C03 20	AIVH 20	C03 26	AIVH 26	C03 32	AIVH 32	D3 38	AI 38	D3 44	AI 44	18
22		— —	E1 8	— —	C5D 14	— —	C5D 20	— —	C5D 26	— —	C5D 32	— —	E1 38	— —		— —	22
26		AW 2	E2 8	AW 8	C6D 14	— —	C6D 20	— —	C6D 26	— —	C6D 32	— —	E2 38	AW 37		AW 44	26
30		— —	E3 8	— —	D7 14		D7 20		D7 26		D7 32	AW 32	E3 38	— —		— —	30
34			E4 8		D8 14		D8 20		D8 26	C8D 26	D8 32	— —	E4 38				34
38			E5 8		D9 14		D9 20		D9 26	C9D 26	D9 32		E5 38				38
42	D2 3	BIW 3	D2 9	BIW 9	D2 15	BIV 15	D2 21	BIV 21	D2 27	BIV 27	D2 33	BIV 33	D2 39	BIVW 39	D2 45	BIW 45	42
46	D1 3		D1 9		C02 15		C02 21		C02 27	AW 27	C02 33		D1 39		D1 45		46
50	D3 3	AI 3	D3 9	AI 9	C03 15	AI 15	C03 21		C03 27	— —	C03 33	AI 33	D3 39	AI 39	D3 45	AI 45	50
54		— —	E6 9	— —	C8D 15	— —	C7D 21	AI 21	C7D 27	AI 27	C7D 33	— —	E6 39	— —		— —	54
58		WEFA 1	E7 9		C9D 15		C8D 21	— —	C8D 27	— —	C8D 33		E7 39				58

Hrs Mins	02 UT CH1	02 UT CH2	05 UT CH1	05 UT CH2	08 UT CH1	08 UT CH2	11 UT CH1	11 UT CH2	14 UT CH1	14 UT CH2	17 UT CH1	17 UT CH2	20 UT CH1	20 UT CH2	23 UT CH1	23 UT CH2	Hrs Mins
2		— —	E8 9			WEFA 3	C9D 21		C9D 27		C9D 33		E8 39				2
6			E9 9			— —							E9 39				6
10	D2 4	BIW 4	D2 10	BIW 10	D2 16	BIVW 16	D2 22	BIVW 22	D2 28	BIVW 28	D2 34	BIVW 34	D2 40	BIW 40	D2 46	BIW 46	10
14	D1 4	TEST 4	D1 10	ADMN 0	C02 16	TEST 0	C02 22	ADMN 0	C02 28	TEST 4	C02 34	ADMN 0	D1 40	TEST 0	D1 46	ADMN 0	14
18	D3 4	AI 4	D3 10	AI 10	C03 16	AIVH 16	C03 22	AIVH 22	C03 28	AIVH 28	C03 34	AIVH 34	D3 40	AI 40	D3 46	AI 46	18
22	TEST 0	— —	ADMN 0	— —	TEST 4	— —	ADMN 0	— —	TEST 0	— —	ADMN 0	— —	TEST 4	— —	ADMN 0	— —	22
26						— —		— —		— —		— —		WEFA 6			26
30														— —			30
34	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	34
38	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	RANG 0	38
42	D2 5	BIW 5	D2 11	BIW 11	D2 17	BIV 17	D2 23	BIV 23	D2 29	BIV 29	D2 35	BIV 35	D2 41	BIW 41	D2 47	BIW 47	42
46	D1 5		D1 11		C02 17		C02 23	AV 23	C02 29		D1 35		D1 41		D1 47		46
50	D3 5	AI 5	D3 11	AI 11	C03 17	AI 17	C03 23	— —	C03 29	AI 29	D3 35	AI 35	D3 41	AI 41	D3 47	AI 47	50
54		— —	E1 11	— —	TEST 4	— —	E1 22	— —		— —	E1 34	— —		— —	E1 47	— —	54
58		CTH 0	E2 11		TEST 4	CTH 0	E2 22	— —		CTH 0	E2 34			CTH 0	E2 47		58

Table 1. Prediction Chart.
June 1987 Maplin Magazine

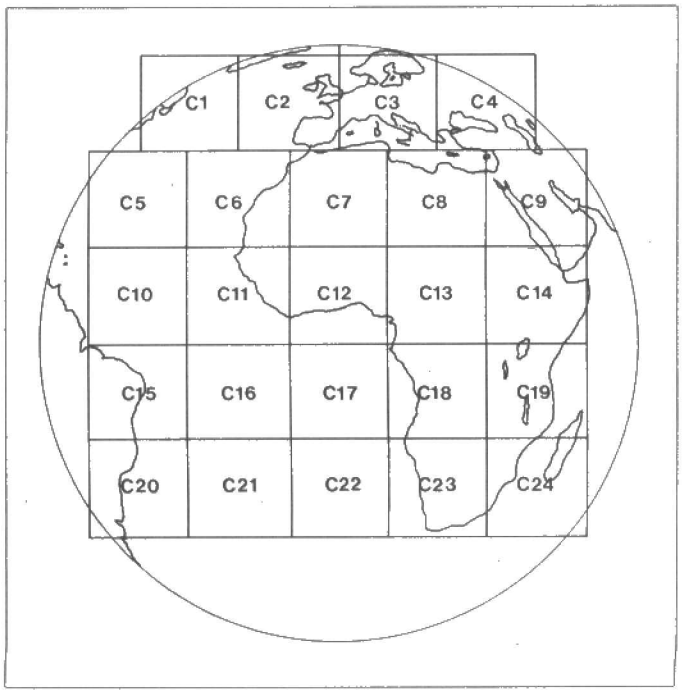


Figure 6. WEFAX visible formats.

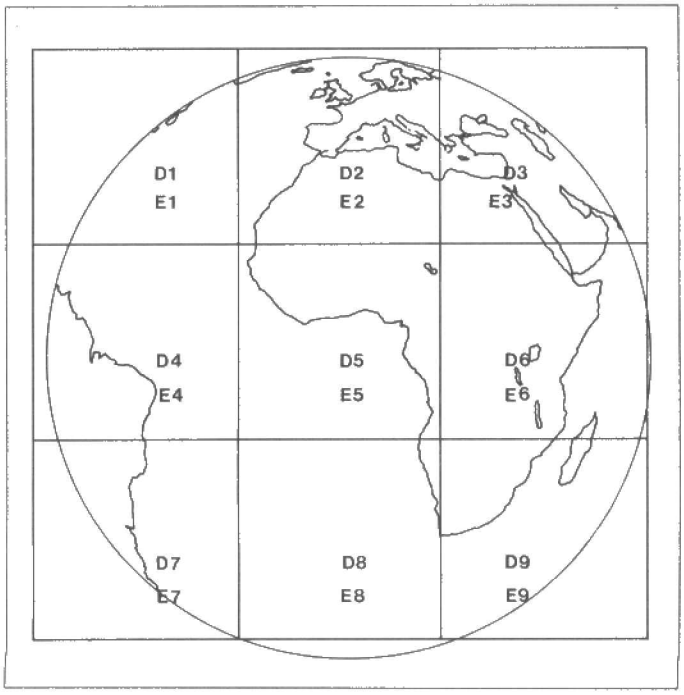


Figure 7. WEFAX IR (formats D) and WV (formats E).

transmitted by Meteosat are preceded by a 5 second burst of peak white signal, the Input Level control on the Decoder should be adjusted to give a full scale reading on the level meter during this tone.

Types of Pictures

Meteosat transmits the following three types of picture:

1. Visible (C format).
2. Infra-red (D format).
3. Water vapour (E format).

All pictures include date, time and format information and by using the maps shown in Figures 6 and 7, as well as Table 1, it is possible to identify the area of the Earth covered by the picture being received. Thus the visible image that covers the largest area of the British Isles is labelled C02. (An infra-red picture of the same area would be labelled C2D).

Channel 1 also transmits test pictures and administrative (ADMN) information. Channel 2 transmits pictures of the whole of Earth's disk (TOT) and also meteorological charts (WEFA).

Information about Meteosat and NOAA satellites may be obtained by calling UK Weatherwatch on 0256 83448, between 1715 and 0845, Monday to Friday or all day Saturday and Sunday.

Final Installation

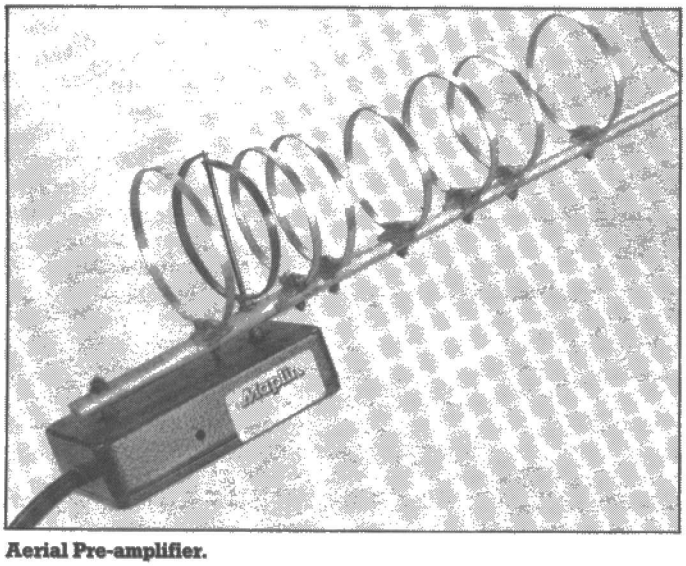
The aerial may be attached permanently to a standard television aerial lashing kit in a convenient position that enables the sighting requirements to be met, but bear in mind that for the final positioning it is best to adjust the aerial direction and angle whilst monitoring the signal strength on the Receiver.

The Down Converter may be mounted up to 4 metres from the aerial; this could enable it to be located inside a building but if this is not possible the unit should be installed in a weather-proof box (YM92A). Cable entry should be at the bottom of the box and any gaps around the cables sealed with silicon rubber (YJ91Y). Avoid locations where the Down Converter may get too hot and mount it in a shady position if possible.

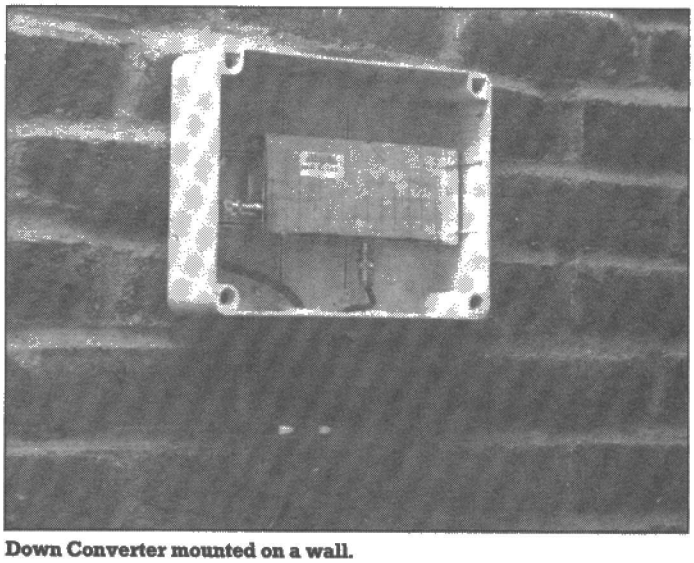
The down lead from the Down Converter to the Receiver should be kept as short as possible to minimise signal losses, although the system has been found to work well with feeders of 15 metres and over. Avoid running the down lead close to sources of electrical interference such as computers, printers, disk drives or video monitors. Longer down leads may be used by inserting an inline 137.5MHz amplifier close to the Down Converter. This extra unit will also help where high levels of interference (at VHF) cannot be avoided. (Details next issue.)

As a matter of routine, a regular check should be made on all external units and the aerial elements should be cleaned from time to time, taking care not to damage the protective varnish applied during construction.

continued →

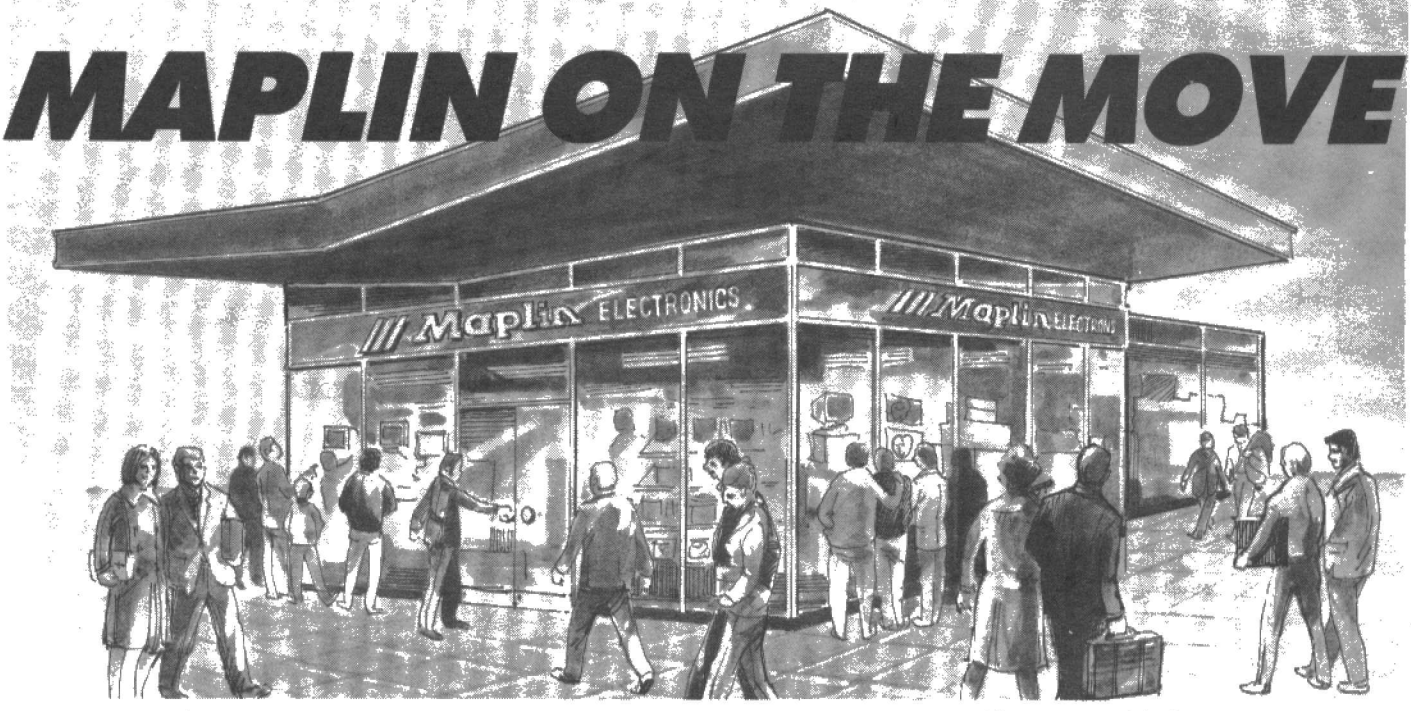


Aerial Pre-amplifier.



Down Converter mounted on a wall.

MAPLIN ON THE MOVE



Due to a forthcoming redevelopment of the Perry Barr shopping centre, Maplin have been forced to find new premises from which to serve their Birmingham customers. Having to move from one shop to another is inconvenient at the best of times for both Maplin and our customers, but we believe this move should be recognised as an advantage, as it provides the company with an opportunity to modernise the sales approach at Birmingham.

As soon as we became aware that Maplin would need to find new premises, the hunt began for a new site which needed to be reasonably close to the current shop to ensure that the staff and customers suffered the least inconvenience possible. Well, we are proud to say that we think an excellent shop has been found which will admirably serve the West Midlands area. Only 2 or 3 miles from Perry Barr, the new Birmingham shop is a short distance from Spagetti Junction on the M6. The site is on the southern end of Sutton New Road, and only a few steps from the High Street in Erdington.

While looking for new premises, one of the prime considerations was that suitable parking should be available within the vicinity. At Erdington we have acquired a shop with an adjoining private car park with up to 50 spaces. Naturally, we hope that the free, convenient access will contribute to the new stores success, but to make the store even more worth a visit we will be changing to the self selection sales format which has become so popular with both the Southend and Manchester customers.

At present it is hoped that the new shop will start trading on Tuesday 16th June, with the Perry Barr branch closing down on the preceding Saturday, 13th June. Although we hope the changeover goes smoothly and according to plan, we recommend that if you are intending to travel to the Birmingham shop around the middle of June, then a telephone call might well be worth considering, just in case any unforseen circumstances speed up or delay the move. The telephone number of our current shop is 0213567292, and providing the Post Office doesn't let us down the new number will be 0213848411.

In the next issue we will try and include some pictures of the new shop, but in the meantime we hope those customers who currently visit Perry Barr are not inconvenienced too much and we look forward to seeing you at Erdington.

Hammersmith Shop Refit

Following close on the heels of the new Birmingham shop, Maplin have decided to refit the Hammersmith branch, bringing it in line with the company's move towards a more modern shopping environment. The self selection shops provide customers with an opportunity to browse amongst the products and see the things which until recently have been just a picture on the Maplin catalogue pages.

Unfortunately, because of some essential building work, we think it will be necessary for the Hammersmith branch to close for a few days. Naturally, we will wish to keep this inconvenience to customers to an absolute minimum. Providing everything goes to plan we will be commencing this work on the 30th June, which means the shop will be closed for at least the first week of July, but possibly the first two weeks. We suggest, if you are contemplating a long journey to the shop, around the beginning or middle of July, that you give the Hammersmith shop staff a ring to ensure the shop is open for business. Finally we apologise to all customers inconvenienced at this time, and hope you will all visit us again when the work is complete.

CHANNEL SWITCHING UNIT PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,12	1M	2	(M1M)
R2	2M2	1	(M2M2)
R3,4,5	100k	3	(M100K)
R6,7,8,9,13	10k	5	(M10K)
R10,11	1k	2	(M1K)
CAPACITORS			
C1,8	180nF Poly Layer	2	(WW44X)
C2,10	2n2F Monores	2	(RA40T)
C3	150nF Poly Layer	1	(WW43W)
C4,5	100nF Minidisc	2	(YR75S)
C6	10nF Minidisc	1	(YR73Q)
C7	560nF Poly Layer	1	(WW50E)
C9	22μF 16V PC Electrolytic	1	(FF06G)
SEMICONDUCTORS			
IC1	40106BE	1	(QW64U)
TR1,2	BC327	2	(QB66W)
TR3	BC337	1	(QB68Y)
D1-D8	1N4148	8	(QL80B)
L1,2	1mH Choke	2	(WH47B)
LED1,2	Red LED	2	(WL27E)
MISCELLANEOUS			
	Veropin 2145	1 Pkt	(FL24B)
SK1	HQ Coax Socket	2	(FE10L)
RL1	Micro-min Relay 12V	1	(BK47B)
S1	Sub-min Toggle Switch D	1	(FH03D)
TB1	Minicon Plug 6-way	1	(YW12N)
	Minicon Socket 6-way	1	(YW28F)
	Minicon Terminal	6	(YW25C)
	LED Clip	2	(YY40T)
	Case DCM3007	1	(LH72P)
	Channel Switch PCB	1	(GD54J)
	Channel Switch Front Panel	1	(FP76H)
	6BA C/snk Head Screw ½in.	1 Pkt	(BF12N)
	6BA Shake Washer	1 Pkt	(BF26D)
	6BA Nut	1 Pkt	(BF18U)
	6BA Spacer ½in.	1 Pkt	(FW33L)
	10-way Ribbon Cable	1 Mtr	(XR06G)
OPTIONAL			
	HQ Coax Plug	2	(FD85G)
	Low-loss Coax White	As Reqd	(XR87U)

A complete kit of all parts, excluding optional items, is available for this project:
Order As LM26D (Channel Switching Unit Kit) Price £17.95
The following items included in the above kit list are also available separately, but are not shown in the 1987 catalogue:
Channel Switch PCB **Order As GD54J Price £2.95**
Channel Switching Front Panel **Order As FP76H Price £2.95**

MACHINE CODE PROGRAMMING WITH THE Z80

Z80

by Graham Dixey C.Eng., M.I.E.R.E. Part Seven

The Z80 microprocessor chip has associated with it a number of peripheral chips that allow it to communicate, in various ways, with a variety of different devices, e.g. keyboards, displays, printers and so on. Two of the most useful form the subject of this article. A proper understanding of how to use their facilities is essential to getting the most out of the Z80 in connection with control applications.

The Z80 PIO

This member of the Z80 family provides two 8-bit, TTL compatible, parallel input-output ports that are capable of being controlled by software so as to be configured in various ways. Interrupt logic is also included. Figure 1 shows both the pin-out for this chip and its block diagram. The ports are known as Port A and Port B and there are four modes in which they can operate. Data transfers between the CPU and the PIO make use of separate input and output registers, known collectively for programming purposes as the Data Register (DR); the control registers associated with each port are also known collectively to the programmer as the Control Register (CR). The PIO operating modes are:

Mode 0: As an 8-bit output port, with 'handshaking'.

Mode 1: As an 8-bit input port, with 'handshaking'.

Mode 2: As a bi-directional port (applies to Port A only), a mode in which the port responds to both input and output commands. It is used where the PIO is connected to an external input-output bus, as in data-logging. Handshaking is provided.

Mode 3: In the 'bit' mode, in which all bits of either port may be either inputs or outputs. No handshaking.

Interrupt Control

An interrupt may be generated either as the result of some input or on the successful completion of an output transfer. Daisy-chaining is possible and is shown in Figure 2, where the PIO is one of a number of peripheral chips in the 'daisy chain'. To effect the action of this chain, there is an input interrupt line IEI, (Interrupt Enable Input) and an output interrupt line IEO, (Interrupt Enable Output). If interrupts to a peripheral are enabled the Interrupt Enable line is high but, if an interrupt is in progress anywhere in the chain then that particular chip takes its IEO line low, thus disabling the following chips in the daisy chain. In Figure 2 peripheral B has an interrupt in progress and has disabled the following chips, C and D. This establishes an interrupt priority structure as discussed in Part Six.

Initialising the Ports

Before use can be made of the ports they must be 'initialised', i.e. set up for the required modes. This is achieved by writing a segment of program right at the beginning. For either Port A or Port B this must specify the following conditions:

(a) The operating mode to be used.
(b) If 'bit' mode is selected, which bits are to be outputs and which are to be inputs.
(c) Whether interrupts are to be used or not.
(d) The interrupt conditions.
(e) The interrupt table address low byte, which forms the interrupt vector together with the contents of the Z80 I register (see Part Six).

It is obviously necessary for the PIO to be able to distinguish between data which forms a command for setting up and an actual data word to be transferred. This is carried out by means of the control line C/D select (pin 5 of the PIO). When this is high the data is a set-up command word and when it is low it is data. The easiest way to select C/D high or low is to feed it from one of the address lines such that different operands are used for the OUT command in the COMMAND and DATA cases, i.e. the latter have separate port addresses. In a similar fashion the A/B select line (which selects either Port A or Port B) is connected to an address line, so that the

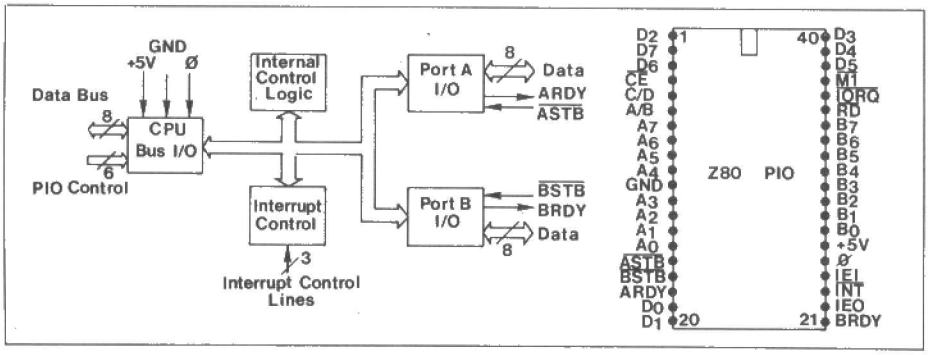


Figure 1. The Z80 PIO block diagram and pin-out.

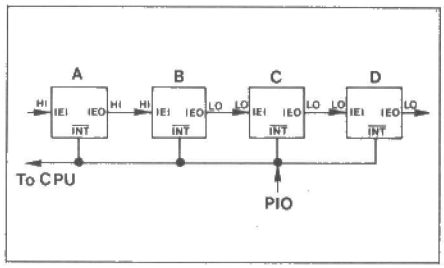


Figure 2. Daisy-chaining the PIO.

ports have separate addresses; this line is high when Port A is selected and low when Port B is selected. In practice the following arrangement can be used for addressing the PIO:

(i) The A/B select line is taken to A_0.

(ii) The C/D select line is taken to A_1.

(iii) Address lines A_2 to A_7 are decoded to select the PIO (CE pin of PIO).

The following examples should make this clear:

(a) Any port address with $A_0 = 1$ and $A_1 = 1$ will select a 'command word to Port A', e.g. &07.

(b) Any port address with $A_0 = 1$ and $A_1 = 0$ will select 'data to Port A', e.g. &05.

(c) Any port address with $A_0 = 0$ and $A_1 = 1$ will select 'command word to Port B', e.g. &06.

(d) Any port address with $A_0 = 0$ and $A_1 = 0$ will select 'data to Port B', e.g. &04.

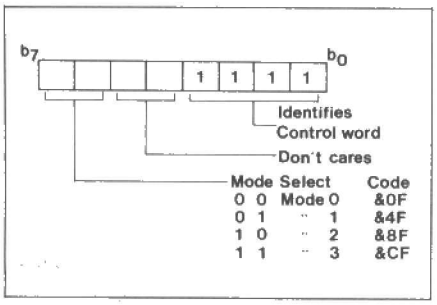


Figure 3. The PIO Control Word for Mode Selection.

Now to look at the content of the commands used to initialise the ports according to the list above. The operating mode required is established by bits 6 and 7 of the Control Word. Figure 3 shows the form of the Control Word and tabulates the bit values needed for each of the four modes.

As an example, suppose it is required to initialise Port A as an input port and Port B as an output port; the program segment required for this initialisation, in assembler, would be:

```
LD    A,&4F   ; Get code for input
                mode (control word).
OUT   &07     ; Send to Port A
                Control Register.
LD    A,&0F   ; Get code for output
                mode (control word).
OUT   &06     ; Send to Port B
                Control Register.
```

This is straightforward enough, but suppose that Port B was actually to operate in the 'bit' mode. It is now necessary to define which bits of the port shall be inputs and which outputs. This requires a second control word to be sent. The bits of this control word must have a 1:1 relationship with the bits of the port concerned. A logic 1 in the control word sets up the corresponding bit to an input while a logic 0 sets it to an output. For example, if bit 7 of the control word is logic 1, then bit 7 of the port will be an input line, and if bit 3 of the control word is logic 0 then bit 3 of the port will be an output line, and so on. Those familiar with the 6522 VIA, the interface chip for the 6502, will appreciate that this is the exact opposite situation. It's actually easier to remember since one readily identifies 1 with Input and 0 with Output.

Suppose that the lower five bits, bits 0-4 inclusive, are to be inputs and the top three bits, bits 5-7 inclusive, are to be outputs, then the control word will be 00011111 = &1F. Thus, to initialise Port B in the bit mode with this particular bit pattern, the following program would be needed:

```
LD    A,&CF   ; Get code for bit
                mode.
OUT   &06     ; Send to Port B
                Control Register.
LD    A,&1F   ; Load A register with
                required bit pattern.
OUT   &06     ; Send to Port B
                Control Register.
```

Before going on to discuss how to program the PIO for interrupts, it is as well to understand what is meant by 'handshaking'. Handshaking is the rather colourful term to describe a means of making the slow speed of most peripherals compatible with the high speed of a microprocessor. To put this into perspective, take the example of a typical dot-matrix printer with a speed of 80 c.p.s. (characters per second). Compared with a human typist plodding along at a mere 40 words/minute, this seems ultra fast. After all, it only takes 12.5ms to print out a single character! However, 12.5ms is 12,500 micro-seconds and if 4 micro-seconds per instruction is allowed (and that's being generous), it is obviously possible to execute 3,125 Z80 instructions in the time of a single printer character. When a peripheral operates at a totally different speed from the microprocessor, it is said to operate 'asynchronously'.

In order to operate handshaking, each port has two handshake lines, a READY line and a STROBE, known as ARDY and ASTB; BRDY and BSTB, for the two ports respectively. They are used as follows:

STROBE: This is an output from the peripheral that either acknowledges data received from the PIO or latches data into the PIO input register.

READY: This is an output from the PIO that either tells a peripheral that it has data for it or tells the peripheral that the PIO's input register is empty and it is waiting for another data byte.

Some idea of the role of these signals may be seen from the simplified timing diagrams of Figure 4.

Taking input handshaking first, the peripheral starts the ball rolling by placing its data on the input port and then taking the STROBE line low; the data is then 'latched' into the port. As the STROBE signal ends, returning to logic 1, the READY line goes low, generating an interrupt. The CPU now reads the data input to the port and signals to the peripheral that it has done so by using the end of the READ signal to take the READY line high again. This signals to the peripheral that it can now send another data byte.

Now consider the output case. At point A, WR goes low, indicating the presence of data to be latched into the PIO. When this data appears on the port lines WR goes high, followed by the READY signal also going high, which tells the peripheral that the data is present (point B). The peripheral now accepts the data and generates a short negative-going pulse on the STROBE line to signal this fact. This clears the READY line and generates an interrupt.

With bi-directional operation there is obviously a problem since this mode requires 'four' handshake lines, two for inputs and two for outputs. The only way to obtain these four lines is to use both READY lines and both STROBE lines for

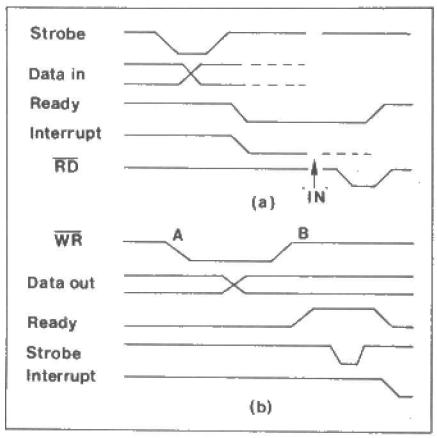


Figure 4. Simplified PIO Timing Diagrams for Handshaking, (a) on inputs, (b) on outputs.

ports A and B but use them all for just one port, Port A. Thus, ASTB and ARDY are used as the output handshake lines, while BSTB and BRDY are used as the input handshake lines. This imposes the limitation that, when Port A is being used in this mode, Port B can only be used in the bit mode, since this requires no handshaking.

As far as the latter mode is concerned, any bit pattern at the port is the sum total of all the input and output lines together. It is possible to generate an interrupt by 'recognising' a given bit pattern.

The Z80 PIO usually uses the Z80 Mode 2 type of interrupt, in which the I register of the Z80 is loaded with the high byte of the interrupt vector and the PIO supplies the low byte; there is one restriction on this low byte and that is, that bit zero must always be a '0', since this is the means by which the PIO recognises that this control word is actually part of the interrupt vector. Thus, in addition to sending a control word that specifies the mode, it is also necessary to send an Interrupt Vector Word.

Whether interrupts are enabled or disabled depends upon another control word, known as the Interrupt Control Word, shown in Figure 5. The low nibble of this word is always 0111 binary (&07) to identify the byte as the Interrupt Enable Word. The highest bit, bit 7, is used to enable or disable interrupts such that:

When bit 7 = 0, interrupts are disabled.
When bit 7 = 1, interrupts are enabled.

This leaves three bits b_4 - b_6, which are only used in Mode 3 and whose functions are as follows:

Bit 4 specifies whether a 'mask' word follows (=1) or not (=0).

Bit 5 specifies whether the input lines to be monitored will generate an interrupt if they are all logic 0 (b_5 = 0) or all logic 1 (b_5 = 1).

Bit 6 allows the programmer to decide whether all the bits of the specified bit pattern have to be present to initiate an interrupt (AND operation) or whether just any one of the specified bits being present will generate the interrupt instead (OR operation). The AND operation is selected when the bit is 1 and the OR operation when it is 0.

If Mode 3 is not the mode being used, then the above three bits are of no importance. If it is wished merely to enable or disable interrupts then there is an alternative control word that can be sent. In this alternative word the low nibble is always 0011 (&03) and bit 7 determines whether the interrupts are enabled or disabled in the same way as before. Thus, the control word could always just be either &83 (enabled) or &03 (disabled) since the other three bits are 'don't cares'.

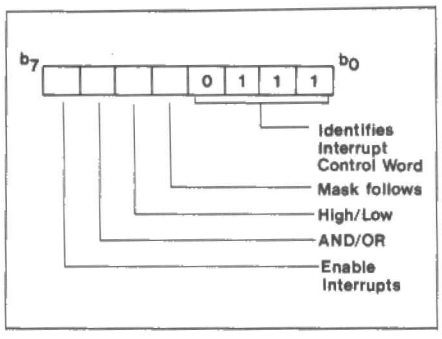


Figure 5. The PIO Interrupt Control Word.

The bit mode is obviously more complex than the others, and so a fully assembled and commented program is shown in Listing 1. The object of this program is to monitor the top four bits of Port A and to generate an interrupt when they are all at logical 1. Notice the number of times that the Control Register CRA has to be written to. Five times in all. Taking these write operations one at a time:

On the first, &CF is the word that selects the bit mode, Mode 3.

On the second, &FF is the Control Word that defines all of the port lines as inputs.

On the third, &C0 is the low byte of the interrupt vector (&5DC0).

On the fourth, &F7 is the Interrupt Control Word. The '7' part of it is fixed and the 'F' part means that all four high bits are 1's, setting - Interrupts Enabled; AND function; Active High, Mask Work Follows.

Finally, the fifth write to CRA sends the Mask Word &0F, which means that the four high bits of an input will be monitored (since these are all zeros in the mask word).

On receipt of any input in which these four bits are all logical 1's, an interrupt will be generated. Lines 19 and 20 are a loop which will be active until this interrupt occurs. When it does so, the interrupt vector, &5DC0, supplied by the I register and the PIO, will direct the program to the Interrupt Service Routine resident at &5D20. A dummy routine is shown here since the actual routine could obviously be almost anything. Nonetheless, it is correctly terminated with EI (to enable further interrupts) and RETI, to pop the stack and return to the main program.

The Z80 Counter Timer Chip (CTC)

The CTC is a particularly useful chip in many control applications because of its ability to handle routine counting and timing operations on its own, once instructed to do so by the Z80. A schematic diagram and pin-out are shown in Figure 6, from which it can be seen that the device contains four 'channels' each of which is able to operate in either timer or counter mode. A schematic for any of the three channels, 0-2, is shown in Figure 7, the only difference between these and the remaining channel, 3, being the absence of a zero count/time out pulse on the latter. All four channels are daisy-chained to establish an interrupt priority, with channel 0 being the highest and channel 3 the lowest. A channel functions as follows.

The principal block is an 8-bit down counter, which has to be loaded with an initial value from the CPU, via the Time Constant Register. This initial value is progressively decremented either at

```
00002  5000  (5000)              ORG   &5000
00003  5000  (0005)    DRA       EQU   &05        ;Data Register A
00004  5000  (0007)    CRA       EQU   &07        ;Control Register A
00005  5000  FB                  EI                ;Enable Z80 interrupts
00006  5001  ED 5E               IM    2           ;Set up Mode 2 interrupts
00007  5003  3E 5D               LD    A,&5D       ;HB of interrupt vector
00008  5005  ED 47               LD    I,A         ;Send it to I Register
00009  5007  3E CF               LD    A,&CF       ;Code for Mode 3
00010  5009  D3 07               OUT   (CRA),A     ;Send to CRA
00011  500B  3E FF               LD    A,&FF       ;Control word
00012  500D  D3 07               OUT   (CRA),A     ;Send to CRA
00013  500F  3E C0               LD    A,&C0       ;LB of interrupt vector
00014  5011  D3 07               OUT   (CRA),A     ;Send to CRA
00015  5013  3E F7               LD    A,&F7       ;Interrupt Control Word
00016  5015  D3 07               OUT   (CRA),A     ;Send to CRA
00017  5017  3E 0F               LD    A,&0F       ;Mask word
00018  5019  D3 07               OUT   (CRA),A     ;Send to CRA
00019  501B  3A 05 00  LOOP      LD    A,(DRA)     ;Get Port A input
00020  501E  18 FB               JR    LOOP        ;Wait for interrupt
00021  5DC0  (5DC0)              ORG   &5DC0       ;Interrupt vector
00022  5D20  (5D20)              ORG   &5D20       ;Interrupt Service Routine
00023  5D20  00        INTVEC.   NOP               ;Dummy routine
00024  5D21  FB                  EI
00025  5D22  ED 4D               RETI
```

Listing 1.

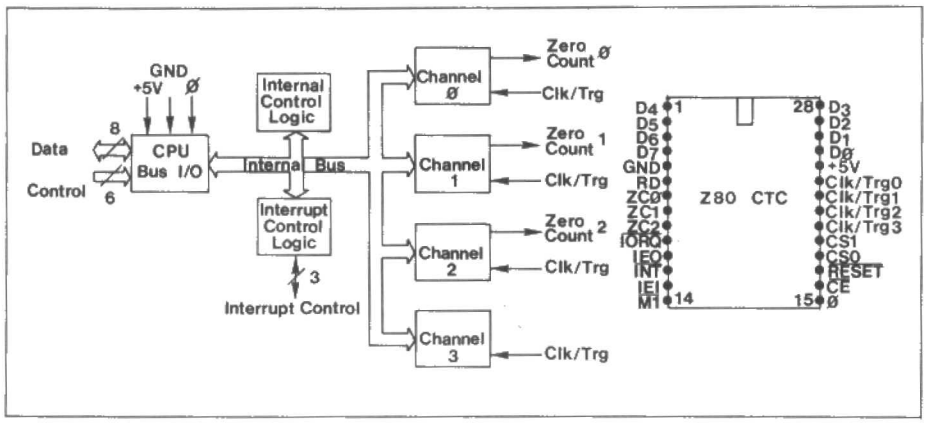


Figure 6. The Z80 CTC block diagram and pin-out.

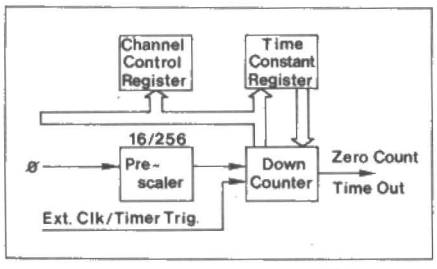


Figure 7. Block Diagram of a CTC Channel.

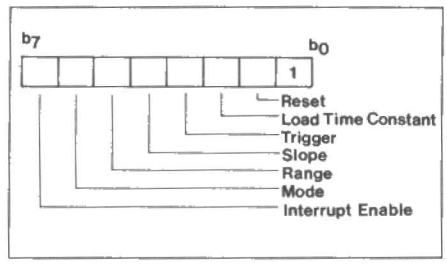


Figure 8. The CTC Control Word for Mode Selection.

clock rate or at a rate determined by some external event. The two alternatives are shown in Figure 7, where it can be seen that the CPU clock rate may be stepped down by a pre-scaler value of either 16 or 256, programmable by the CPU. This is generally used in the timer mode. What happens when the down counter eventually reaches zero is, that an interrupt is generated for whatever purpose you like and the down counter is reloaded from the Time Constant Register. The process keeps on repeating; this is the counter mode of operation.

Another important register is the Channel Control Register (CCR), which exercises control over the mode of operation on receipt of an appropriate control word from the CPU. Each channel has its own CCR; indeed each channel is totally independent of the other three. A channel is selected according to the control signals CS0 and CS1, as follows:

	CS1	CS0
Channel 0	0	0
Channel 1	0	1
Channel 2	1	0
Channel 3	1	1

A channel is selected in practice by giving it an input/output address. For example, if CS0 is connected to address line A_0 and CS1 is connected to address line A_1, then any addresses whose lowest two bits are 00, 01, 10 and 11 could select the four channels. However, to narrow down the choice, as it were, the address lines A_2 - A_7, together with the control line IORQ are decoded to select the CTC chip, to place these channels at four specific, consecutive addresses on the input/output map.

Selecting an Operating Mode

To select an operating mode for a channel it is necessary to write a control word into the channel's control register; to effect this, bit 0 of the word must always be a 1 otherwise it will be mistaken for an interrupt vector. The format of this control word is shown in Figure 8, with the explanation being shown in Table 1.

Loading a Time Constant

If a channel control word with bit 2 set is sent, the CTC will expect the next word to be the time constant to be used in the down counter. This can have a value in the range &01 - &FF, giving the normal denary range 0 - 255, plus &00, which does not signify zero but 256.

Loading an Interrupt Vector

The CTC uses the Z80's Mode 2 for the interrupts and, therefore, as for the PIO, must be supplied with the low byte of the interrupt vector. This byte is loaded by writing into channel 0 with a zero in bit 0 of the word. The situation is complicated by the fact that there is a priority system within the channels of the CTC and each must therefore have its own unique interrupt vector. This need not worry the programmer though; as long as he ensures that bit 0 is zero and supplies bits 3-7, the CTC will supply bits 1 and 2 according to which channel has interrupted. The format of this word, together with the values of bits 1 and 2, is shown in Figure 9.

As an example, suppose that it is required to allocate an interrupt vector for channel 0, then the lowest three bits must all be 0's. One of many possible addresses is &5DF0. This and the next location, &5DF1, would hold the start address for the channel 0 Interrupt Service Routine. Interrupt vectors for the other channels would then automatically be:

Channel 1 &5DF2
Channel 2 &5DF4
Channel 3 &5DF6

All of which can be verified by checking bits 1 and 2 against the table of Figure 9. To set this up it would be necessary to:

(a) Set the Z80 to operate in Mode 2.

(b) Write the interrupt vector word &F0 to the Channel Control Register.

(c) Load the interrupt vectors in memory with the start addresses of the ISR's.

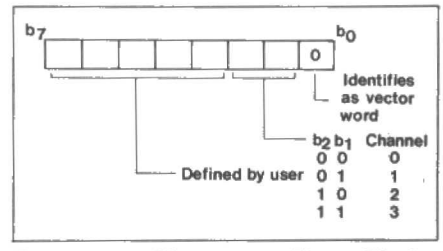


Figure 9. The CTC Interrupt Vector Word.

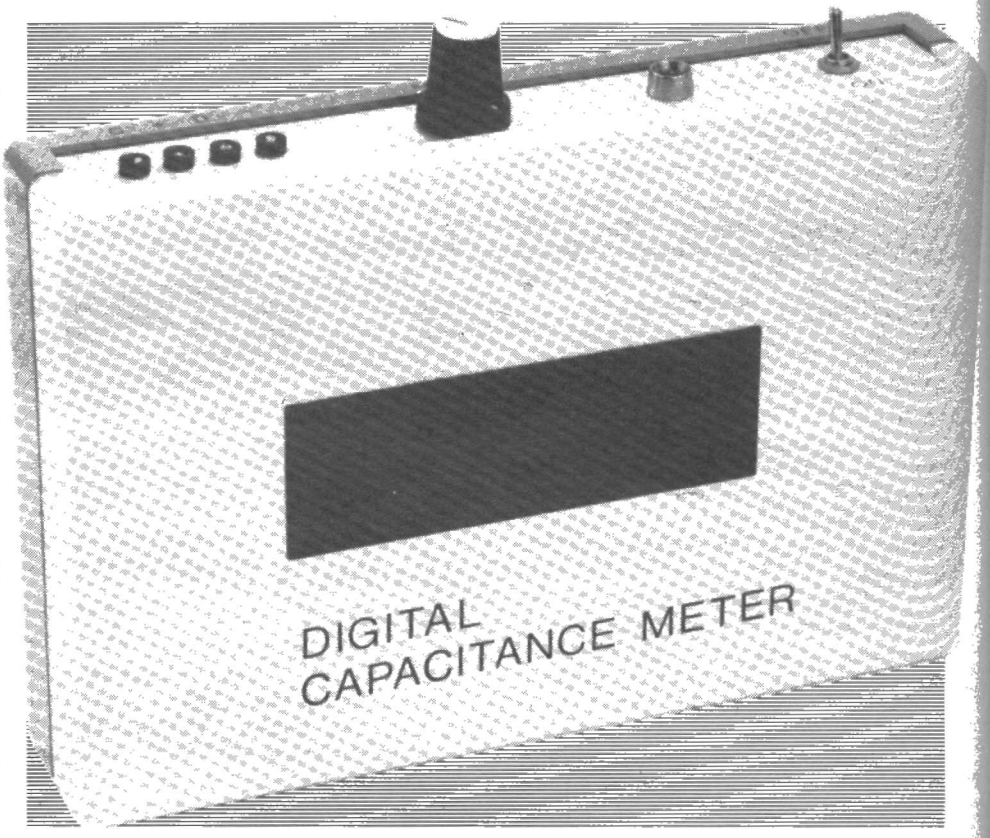
Bit 7 = 0	Channel interrupts disabled.
Bit 7 = 1	Channel interrupts enabled.
Bit 6 = 0	Select timer mode.
Bit 6 = 1	Select counter mode.
Bit 5 = 0	Timer mode only; pre-scaler = 16.
Bit 5 = 1	Timer mode only; pre-scaler = 256.
Bit 4 = 0	Negative edge operation in either mode.
Bit 4 = 1	Positive edge operation in either mode.
Bit 3 = 0	Timer mode only - automatic triggering.
Bit 3 = 1	Timer mode only - CLK/TRG pulse starts timer.
Bit 2 = 0	Timer mode only - no time constant follows.
Bit 2 = 1	Timer mode only - time constant follows.
Bit 1 = 0	Operation continues.
Bit 1 = 1	Software reset.
Bit 0 = 0	Signifies interrupt vector word.
Bit 0 = 1	Signifies control word.

Table 1.

Continued on page 57.

DIGITAL CAPACITANCE METER

by Robert Penfold



Practically every constructional project includes a number of capacitors, and the ability to test these components is a decided assett for any electronics constructor. Unfortunately, testing capacitors properly is something that is beyond the capability of most multimeters and other items of test equipment that are likely to be found in the average amateur electronics workshop. It is possible to make a few rough checks on capacitors using many analogue multimeters, and some modern oscilloscopes have a built-in component tester function that can be used to give some idea of a test capacitor's value, but for accurate measurement of capacitance a proper capacitance meter is required.

This design has a three digit LED display, and it covers five ranges which are as follows:–

Range 1	0 to 9.99nF
Range 2	0 to 99.9nF
Range 3	0 to 999nF
Range 4	0 to 9.99μF
Range 5	0 to 99.9μF

This coverage includes all the common values, but the unit cannot measure very low values of just a few picofarads, or high value electrolytic components. In practice this is not likely to matter too much as very low value components are little used in modern circuits, and large values can be checked by using two components wired in series, as will be explained more fully later in this article. An overflow indicator LED is included so that misleading results are avoided if an unsuitable range is selected. The unit is powered from an internal 9 volt battery, and is in consequence fully portable.

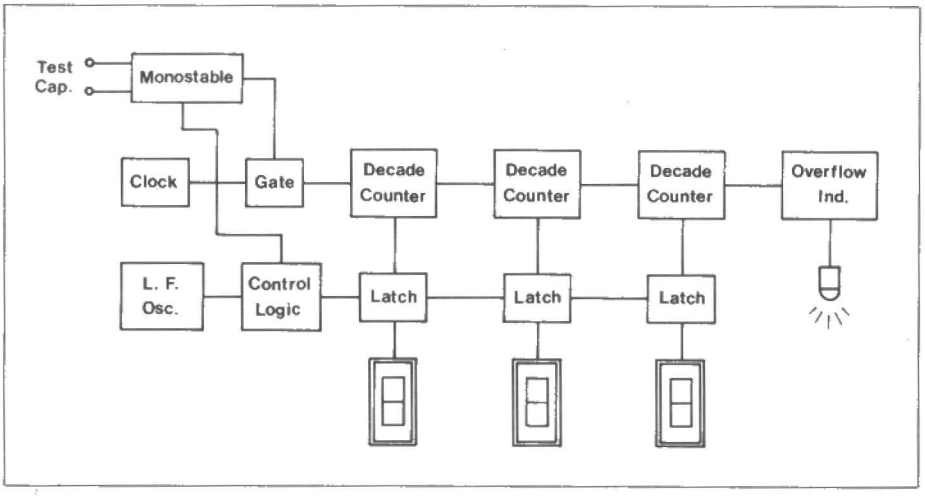


Figure 1. Block schematic.

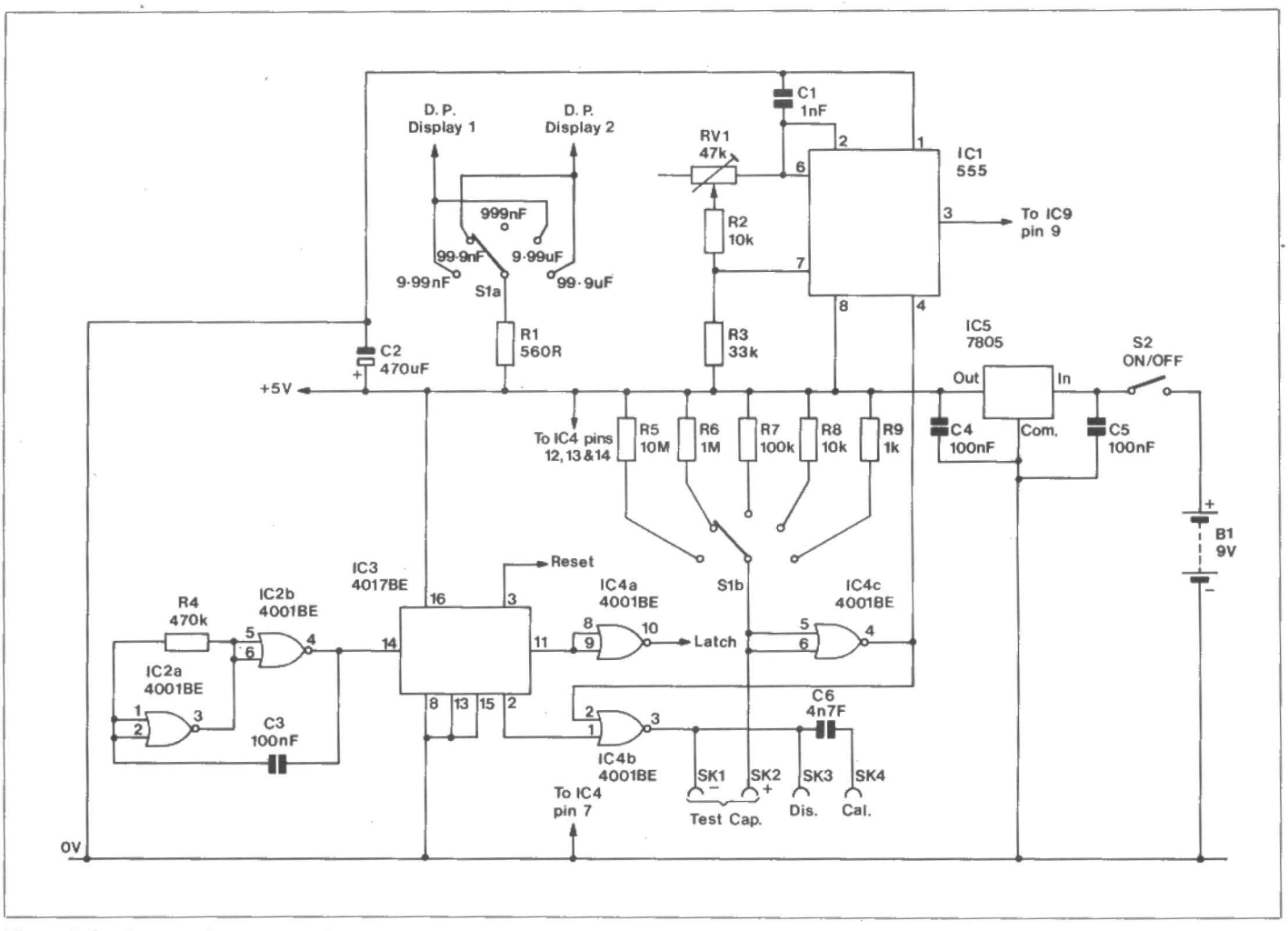
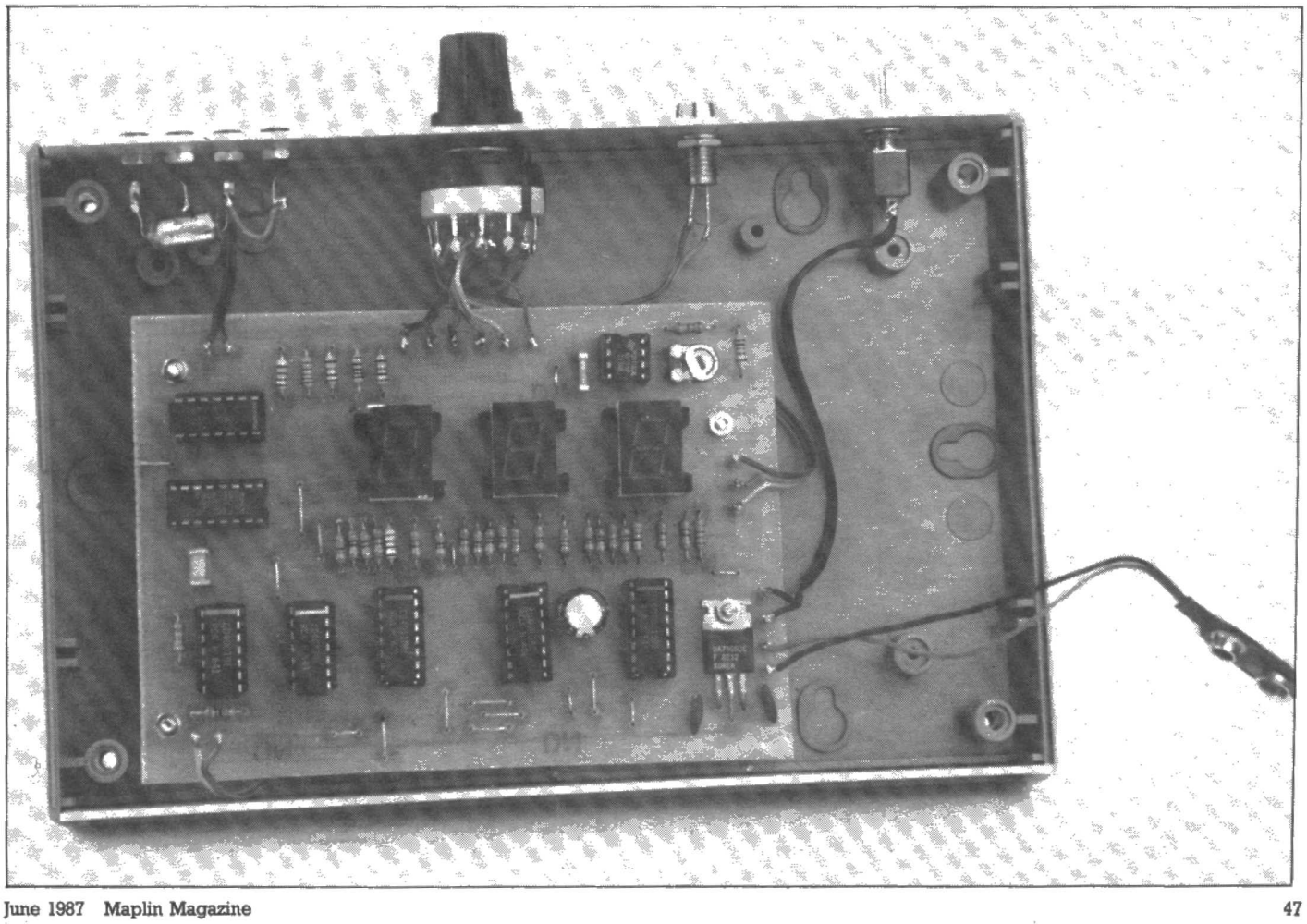


Figure 2. Clock, control and monostable circuit.



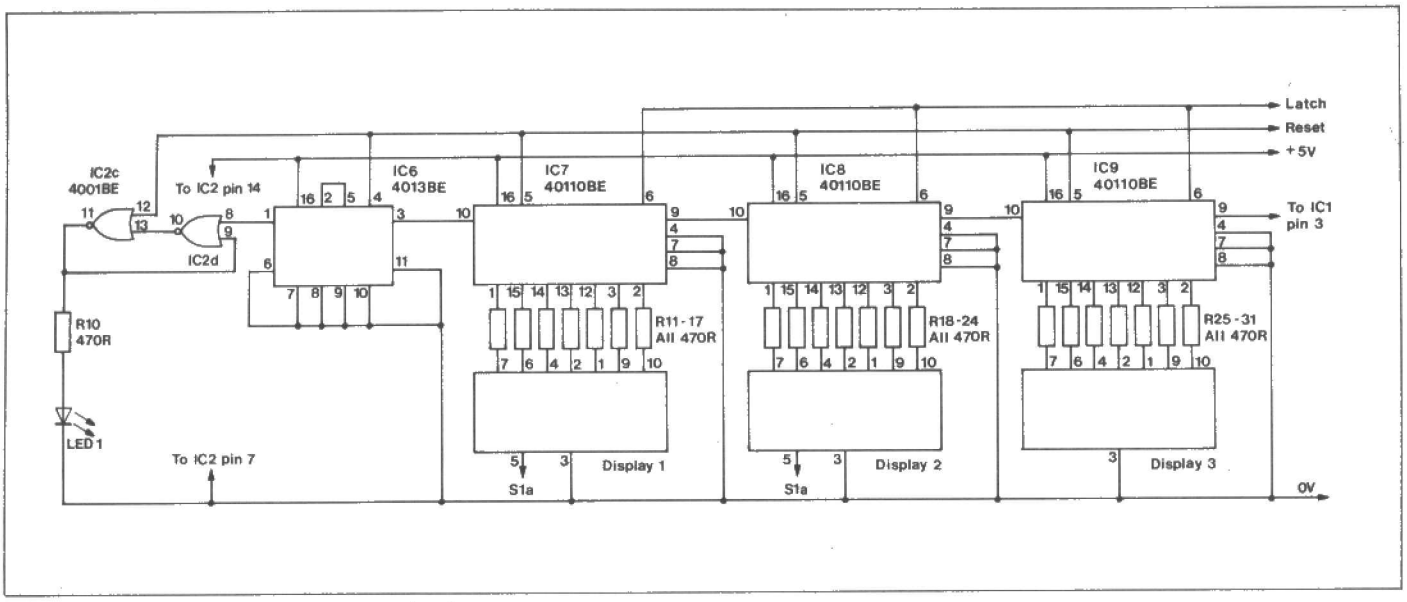


Figure 3. Counter and overflow indicator circuit.

System Operation

In common with most capacitance measuring devices, this one operates by using the test component as the capacitive element in a C-R timing network. In this case the timing network forms part of a monostable multivibrator, and the higher the value of the test component the longer the output pulse of this circuit. There is a linear relationship between the value of the test component and the output pulse duration, and this makes it relatively easy to employ the pulse in controlling a display circuit that gives a reading directly in nanofarads or microfarads (nF or μF). The block diagram of Figure 1 helps to explain the way in which the unit functions.

A low frequency oscillator controls the rate at which readings are taken, and this gives readings at just under one second intervals. The output of the oscillator drives a simple control logic circuit, and this provides pulses that sequence the rest of the circuit correctly. The first operation in the sequence is for a trigger pulse to be sent to the monostable multivibrator, and this then generates an output pulse that is used as the gate pulse for a clock oscillator and a three digit counter circuit. The longer the gate pulse, the higher the count value that the display will reach at the end of the gate pulse, where the count is 'frozen'. In practice, the clock frequency is adjusted so that the display readings are accurate capacitance values. With a three digit counter only a rather restricted range of values can be accommodated with good accuracy, and so the monostable is equipped with five switched timing resistors. These give the unit its five measuring ranges, and enable a wide range of values to be catered for.

The counter circuit is of conventional design, having latches and seven segment decoder/drivers. The value held within the counters is therefore not displayed immediately, but is held in the counters until the control logic circuit provides the latches with a latching pulse. The new value is then displayed, and remains displayed even when the control logic circuit sends a reset pulse to the counter circuit. This reset pulse is essential as it is needed to ensure that the counter starts at '000' when the next gate pulse commences. The point of including the latches instead of driving the decoder/drivers direct from the counters is that it permits a continuous display to be provided. Without the latches the reset and counting action would be displayed, which would give unacceptable results in practice.

If the test capacitor has a value which is beyond the full scale value of the range in use, the counter circuit will go through one or more complete cycles, and will display an erroneous result. To prevent the user from being misled, an overflow indicator circuit is included, and this simply switches on an LED indicator if a complete output cycle is produced by the final decade counter stage. A full output cycle is only produced from this stage if it cycles through a complete 0 to 9 count and then back to zero again.

Circuit Operation

Figure 2 shows the circuit diagram for the clock oscillator, low frequency oscillator, control logic, and monostable stages of the unit. The counter/driver and overflow circuit is shown separately in Figure 3.

Starting with Figure 2, IC5 is a 5 volt monolithic voltage regulator which gives a well stabilised 5 volt output from the 9 volt battery supply. All circuitry is powered from the stabilised 5 volt supply rail. The battery needs to be a fairly high capacity type (such as six HP7 size cells in a plastic holder) as the current consumption of the circuit is quite high at around 85 mA. The current consumption can exceed 100mA when most or all of the display segments are driven, and for this reason a low power voltage regulator is inadequate for the IC5 position.

The low frequency oscillator is based on IC2a and IC2b which are CMOS NOR gates. However, in this circuit they are wired as simple inverters and are used in a standard CMOS astable configuration. Note that the operating frequency of the oscillator is much higher than the frequency at which readings are taken, since ten output cycles are needed from this oscillator in order to complete one reading cycle.

IC3 and IC4a form the control logic block. IC3 is a CMOS 4017BE one-of-ten decoder, and this has ten outputs ('0' to '9') which each go high, in sequence, for a single input cycle. In this circuit output '0' provides the reset pulse to the counters. Output '1' then goes high and triggers the monostable which generates the gate pulse for the clock/counter circuit. Outputs '2' to '8' are unused, and the period during which these go high provides time for the gate pulse to finish and the count to be completed. Output '9' provides the pulse that latches the new reading onto the display, but a negative latching pulse is required. IC4a is therefore used to invert the signal so as to give a suitable pulse. The timing diagram, Figure 4, shows the sequence of events and may help to clarify operation of the unit.

The monostable multivibrator is a conventional CMOS type which is formed from two 2 input NOR gates (IC4b and IC4c). Although a very simple form of monostable, it has characteristics which make it well suited to the present application. It is a non-retriggerable type, and consequently it can provide an output pulse that is shorter than the trigger pulse from IC3. This is important, as with a retriggerable type the minimum display reading would be quite high. The self capacitance of the circuit is quite low, and this is important as a high level of local capacitance would upset the linearity of the circuit, and would give a large minimum display reading. On the prototype the display reads '000' on all five ranges with no test capacitor connected.

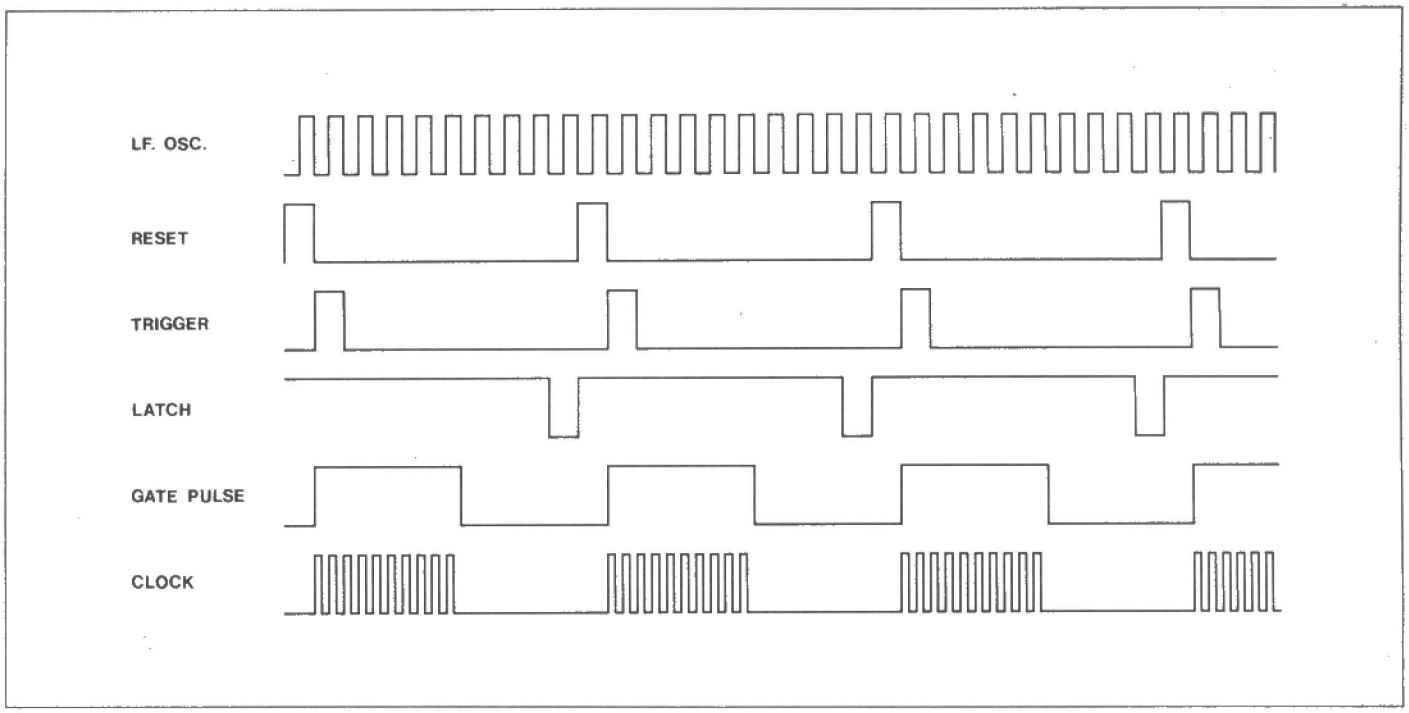


Figure 4. Timing diagram.

R5 to R9 are the range resistors, and by reducing the timing resistance in decade steps the timing capacitance needed for a given reading is boosted in decade increments. Provided the range resistors have a tolerance of 1% or better, this arrangement seems to give consistent results, and there is no need to have each range individually calibrated. R1 and S1a are used to drive the decimal point segment of the appropriate display, except on Range 3 (999nF) where no decimal point indication is needed.

The clock oscillator is a standard 555 astable circuit. RV1 controls the clock frequency, and this is used to calibrate the unit. The output of the monostable drives pin 4 of IC1, and the clock oscillator is only operative during the gate period. This avoids the need for a separate signal gate.

Turning our attention to Figure 3 now, the counter circuit is based on three CMOS 40110BE devices. These are perhaps not the best known of the CMOS logic family, but they are very versatile components which deserve greater usage. They are actually up/down counters with separate clock inputs and carry/borrow outputs. As it happens the ability to operate in a down counter mode is of no value here, and the down clock input is simply tied to the negative supply rail. The three counters are wired in series to give a standard three digit display, with IC9 providing the least significant digit and IC7 furnishing the most significant digit. The 40110BE contains a decade counter, a seven segment decoder, and a latch/display driver circuit. Each chip can therefore replace a standard three chip TTL style counter/driver/latch arrangement. The outputs can directly drive a common cathode seven segment LED display and, unusually for a CMOS logic device, a high drive current is available from each output. Even with a supply potential of just 5 volts it is essential to drive each display segment via a current limiting resistor in order to keep the current consumption of the unit down to a reasonable level.

The 'carry' output of IC7 is fed to the clock input of IC6, which is a dual D type divide by two flip/flop, but in this circuit only one section of the device is utilised. The output of IC6 changes state in the event of an overload, but with a severe overload there could be several output cycles from IC7. Directly driving the LED indicator LED1 from IC6 would not be totally satisfactory, since this output is transitory and the LED might only give one or two brief flashes which could easily be missed. To avoid this the output of IC7 is used to drive a simple set/reset bistable circuit formed from two otherwise unused gates of IC2, and the latch drives LED indicator LED1. Both IC6 and the latch are reset from IC3 so that the overflow circuit starts afresh when a new reading is taken.

Safety First

Simple but important additions to the circuit (in Figure 2) are the two extra sockets at the input (SK3 and SK4) and capacitor C6. The purpose of SK3 is to enable test components to be discharged between SK1 and SK3 prior to connecting them across SK1 and SK2 and making a measurement. This applies only to components which have been in use in a circuit and might contain a residual charge prior to testing. Higher value types which have been used in fairly high voltage circuits are the ones which are most likely to cause problems. Of course, in extreme cases capacitors must be slowly discharged through a 'bleed' resistor before removing them from the circuit. This is as much for your own protection as for that of the capacitance meter, and great care must be exercised when dealing with charged, high voltage components of other than very low values. Building a protection system into the meter input circuit was considered, but it is difficult to produce a really effective circuit that does not impair the performance of the unit. This simple alternative was therefore considered to be the more practical solution to the problem.

C6 is a built-in calibration capacitor. This is not an essential part of the unit, but it is handy when initially calibrating the unit, and therafter it is very useful to have a calibration component that is always immediately available for testing purposes. If a test component gives a slightly erroneous reading it is then just a matter of switching to range 1, connecting SK2 to SK4 to connect C6 into circuit, and then checking that a valid reading is obtained (4.70nF). A word of warning is due here though, and this is simply to point out that the meter itself is only likely to be accurate to within a couple of percent or so, except at values equal to or close to the calibration value. Another point to bear in mind is that the values of capacitors are dependent on temperature and other factors. If a test component should happen to give a reading that is in error by slightly more than its tolerance, this probably means that it is perfectly satisfactory rather than faulty.

Construction

Virtually all the components fit onto the printed circuit board, and details of the board are provided in Figure 5. Construction of the board is not particularly difficult, but there are a few points which should be borne in mind when assembling it. The main point to note is that, apart from IC1 and IC5, the integrated circuits are CMOS types, and

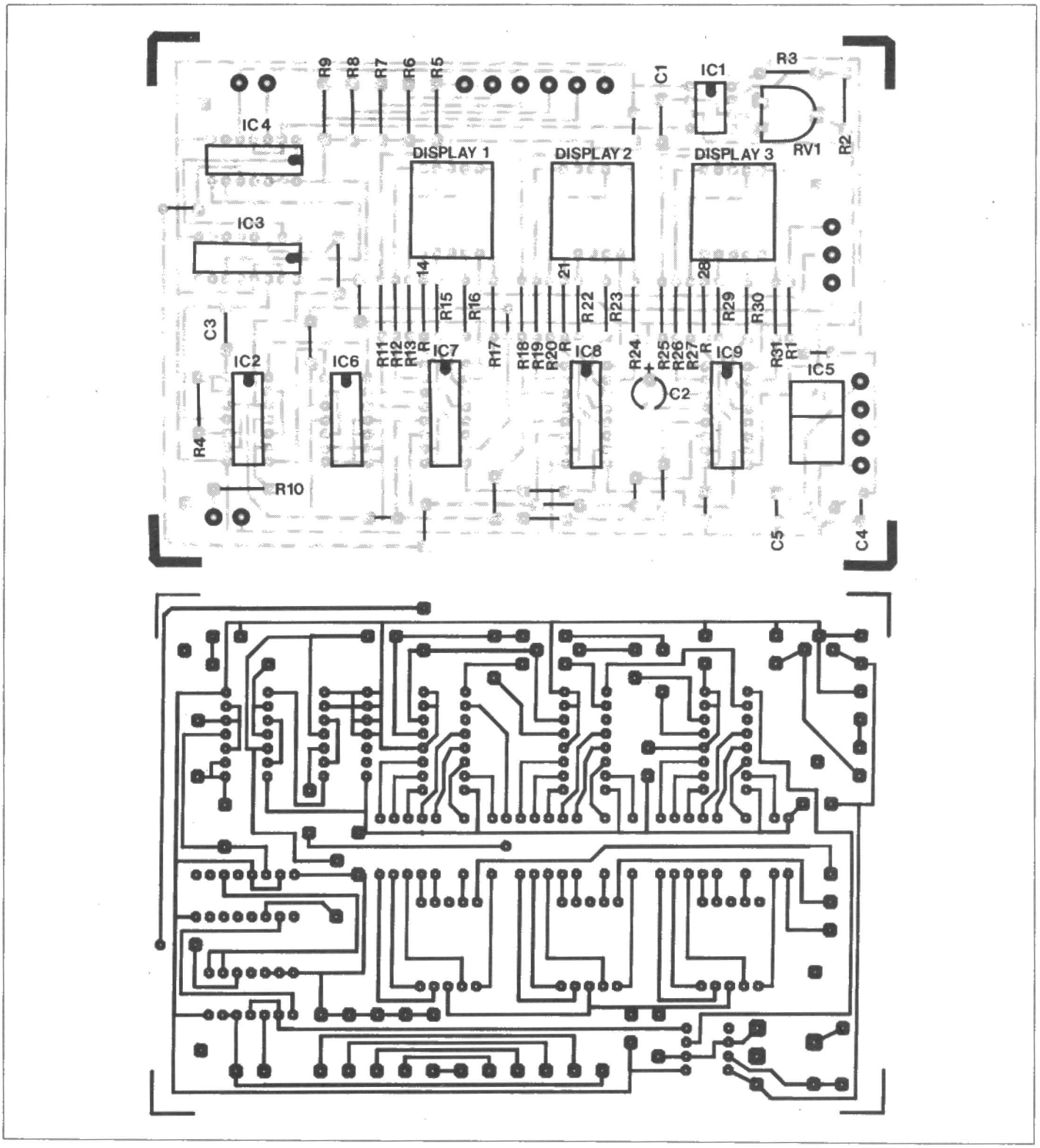


Figure 5. PCB layout and component references.

are therefore vulnerable to damage by static charges. To avoid this they should be fitted in integrated circuit holders, but not be plugged into circuit until the board has been completed and wired to the off-board components (see Figure 6). Until then they should be left in the anti-static packaging. Handle the devices as little as possible when fitting them into the holders, and be particularly careful with the three counter ICs, which are not the cheapest of CMOS devices. If in any doubt, or you are not an experienced constructor, then read the Constructor's Guide leaflet supplied with this kit.

IC5 is mounted horizontally on the board and it is a good idea to use a short 6BA or M3 screw and matching nut to fix it securely to the board.

The three seven segment LED displays are mounted in holders which help to raise them to a suitable height above the surface of the board as well as reducing the risk of heat damage when connecting them. Suitable ten pin holders seem to be unavailable, but it is not difficult to improvise suitable holders from three ordinary 14-pin DIL integrated circuit holders. First the holders are cut in half lengthwise using a hacksaw to give six seven pin SIL types. The pins at each end of the holders are then pushed out using pliers or simply trimmed off using wire clippers. This leaves six 5-pin SIL holders which can be used for the displays. The spacing between the displays is sufficient to make it unnecessary to trim off the excess pieces at each end of the holders.

Pins are fitted to the board at the positions where connections to off-board components will be made. There are a number of link wires (sixteen in fact) and these are made from about 22 s.w.g. enamelled copper wire, or trimmings

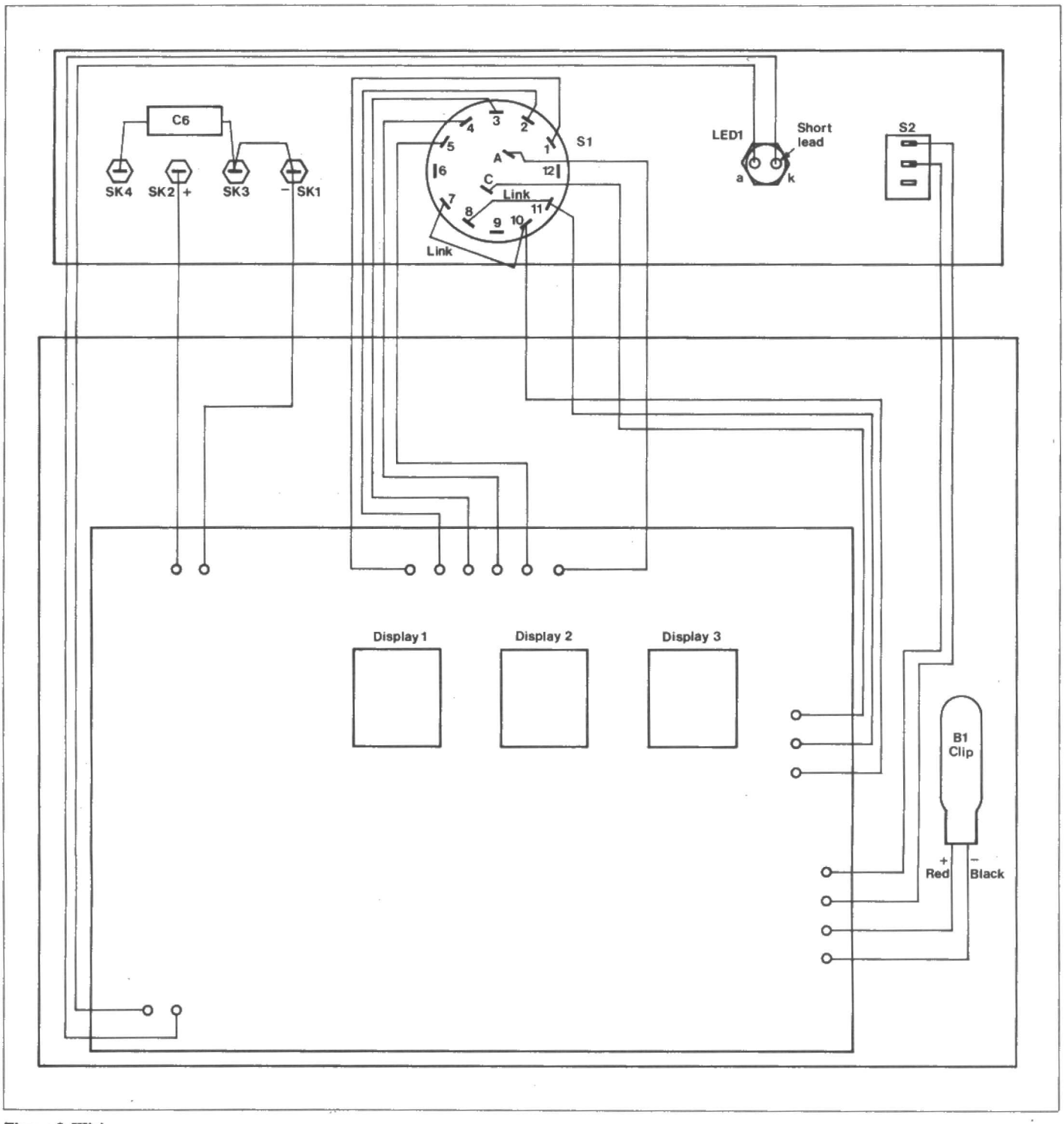
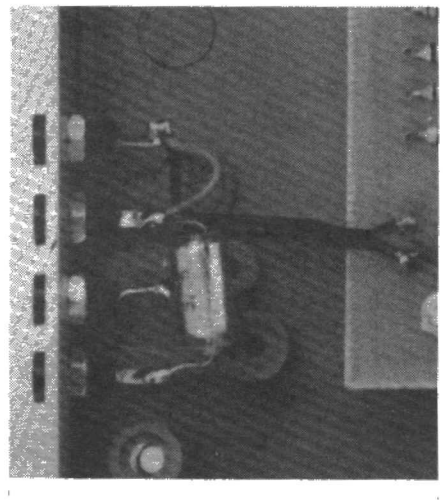


Figure 6. Wiring.

from resistor lead-out wires can be used.

A Verocase having approximate outside dimensions of 205 by 140 by 40 millimetres makes a good housing for this project. It is used vertically with a display window cut in the front panel (which would normally be the top panel), while the controls and sockets are mounted on the top panel (which would usually be the front of the case). The printed circuit board is mounted on the rear panel using one inch long 6BA screws and half inch spacers, which are needed to bring the fronts of the displays close to the display window. The board is positioned well towards the bottom left hand corner of the unit so as to bring the display close to the middle of the front



panel. The display window must obviously be positioned accurately in front of the display, and it can be cut using a fretsaw, coping saw, or a miniature round file. A piece of red display filter is glued in place over or behind the cutout, and any general purpose material is suitable for this. Note that the Maplin display filter material has an anti-glare finish on one surface, and this less reflective surface should be the one that faces forward or outwards.

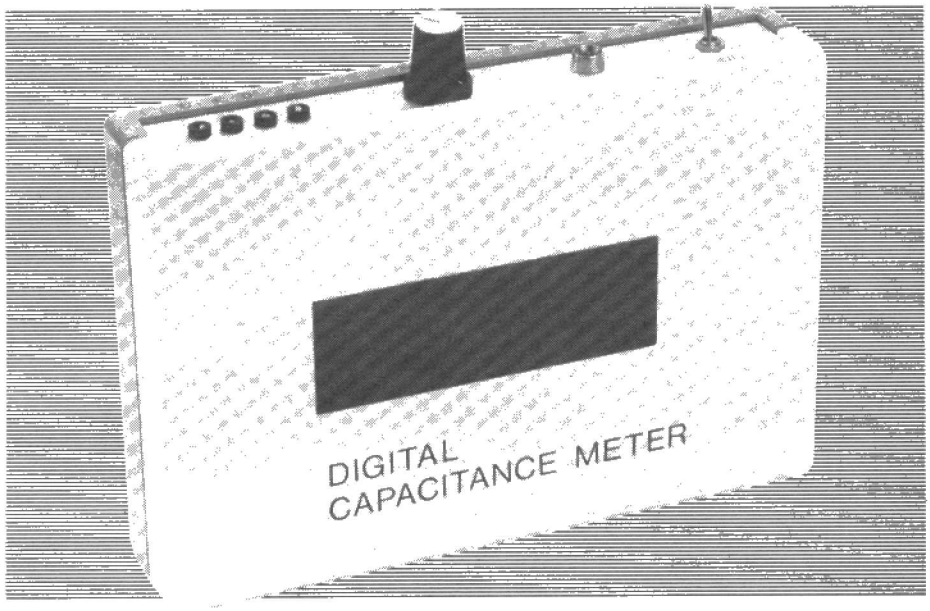
On the prototype SK1 to SK4 are 1 millimetre sockets mounted with about 9.5 millimetres spacing. C6 is mounted direct across SK3 and SK4 so as to minimise stray capacitance, and preserve good accuracy at low readings.

Most capacitors will plug straight into SK1 and SK2 satisfactorily. However, some types, especially miniature printed circuit mounting polyester types will not, and a set of test leads should be made up so that these can be accommodated. All that is needed here is a pair of short insulated leads fitted with 1 millimetre plugs to connect to SK1 and SK2, and small crocodile clips which connect to the component under test.

S1 is a six way switch having an adjustable end-stop which is set for five way operation. Details of the wiring to S1 are shown in Figure 6. LED1 is specified as a panel mounting LED, but if preferred it would not be difficult to utilise the otherwise unused decimal point segment of display 3. If six HP7 size cells in a plastic holder are used as the power source, the connection to the holder is made by way of a standard PP3 style battery connector. It has to be emphasised that a reasonably high capacity battery is needed due to the high current consumption of the circuit, and a small type such as a PP3 is not adequate.

Calibration

In order to calibrate the unit it is necessary to have a close tolerance capacitor of a value that represents about 50 to 100% of the full scale value of one range. Assuming that C6 has been included in the unit and will be used to calibrate it, set the unit to range 1 (9.99nF full scale) and place a shorting link across SK2 and SK4. Then carefully adjust RV1 for the correct display reading of 4.7nF. The unit should then give appropriate readings if it is tried with a range of capacitors, but do not expect



readings to be absolutely spot on. The capacitance meter itself is reasonably accurate, although, as explained previously, it will almost certainly produce small errors. Most capacitors have quite high tolerances though, with few types having an accuracy of better than 5%, and 20% being quite typical. With electrolytic types a tolerance of +50% and −20% is quite normal. Really the inclusion of a third digit in the display is not justified in terms of the required accuracy, but it is useful in that it effectively extends the minimum capacitance which the unit can read by a full decade. If you hold a capacitor in place across the sockets you may well find that the displayed readings steadily increase. This does not indicate a fault in either the capacitor or the capacitance meter, it is simply due to heat from your fingers causing the value of the capacitor to rise slightly. When holding a capacitor in place across SK1 and SK2, always hold the body of the component and do not touch either of the lead-out wires.

High value capacitors can be checked by wiring them in series with a lower value type and then measuring the series capacitance of the two components. For example, a 470μF component could be checked by wiring it in series with 100μF capacitor. The series capacitance is equal to (C1 x C2)/(C1 + C2), which in this example is (470 x 100)/(470 + 100), which gives 47000/570, and a final value of 82.5μF. The capacitors will presumably be electrolytic types, but the polarity of both components is unimportant.

CAPACITANCE METER PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1	560Ω	1	(M560R)
R2,8	10k	2	(M10K)
R3	33k	1	(M33K)
R4	470k	1	(M470K)
R5	10M	1	(M10M)
R6	1M	1	(M1M)
R7	100k	1	(M100K)
R9	1k	1	(M1K)
R10-31	470Ω	22	(M470R)
RV1	47k Hor Sub min Preset	1	(WR60Q)
CAPACITORS			
C1	1nF Poly Layer	1	(WW22Y)
C2	470μF 16V PC Electrolytic	1	(FF15R)
C3	100nF Poly Layer	1	(WW41U)
C4,5	100nF Minidisc	2	(YR75S)
C6	4n7F 1% Polystyrene	1	(BX64U)
SEMICONDUCTORS			
IC1	NE555	1	(QH66W)
IC2,4	4001BE	2	(QX01B)
IC3	4017BE	1	(QX09K)
IC5	μA7805	1	(QL31J)
IC6	4013BE	1	(QX07H)
IC7,8,9	40110BE	3	(QW68Y)
Display 1,2,3	0.5 inch Common Cathode Display	3	(FR41U)
LED1	Panel LED	1	(YY60Q)
MISCELLANEOUS			
S1	6-way 2-pole Rotary Switch	1	(FH43W)
S2	SPST Ultra-Min Toggle	1	(FH97F)
SK1-4	1mm Socket	4	(WL59P)
	8-pin DIL Socket	1	(BL17T)
	14-pin DIL Socket	6	(BL18U)
	Case type 201	1	(LL05F)
	16-pin DIL Socket	4	(BL19V)
	Printed circuit board	1	(GD59P)
	Control knob	1	(YG40T)
	Knob cap	1	(QY03D)
	Battery connector	1	(HF28F)
	Display filter	1	(FR34M)
	Bolt 6BA 1in	1 Pkt	(BF07H)
	Nut 6BA	1 Pkt	(BF18U)
	6BA spacer ¼in	1 Pkt	(FW34M)
	Pin 2145	1 Pkt	(FL24B)

A complete kit of all parts is available for this project:
Order As LM28F (Digital Cap Mtr) Price £29.95
The following item in the above kit list is also available separately, but is not shown in the 1987 catalogue:
Digital Cap Meter PCB **Order As GD59P Price £3.50**

The Story of Radio

by Graham Dixey
C.Eng., M.I.E.R.E.

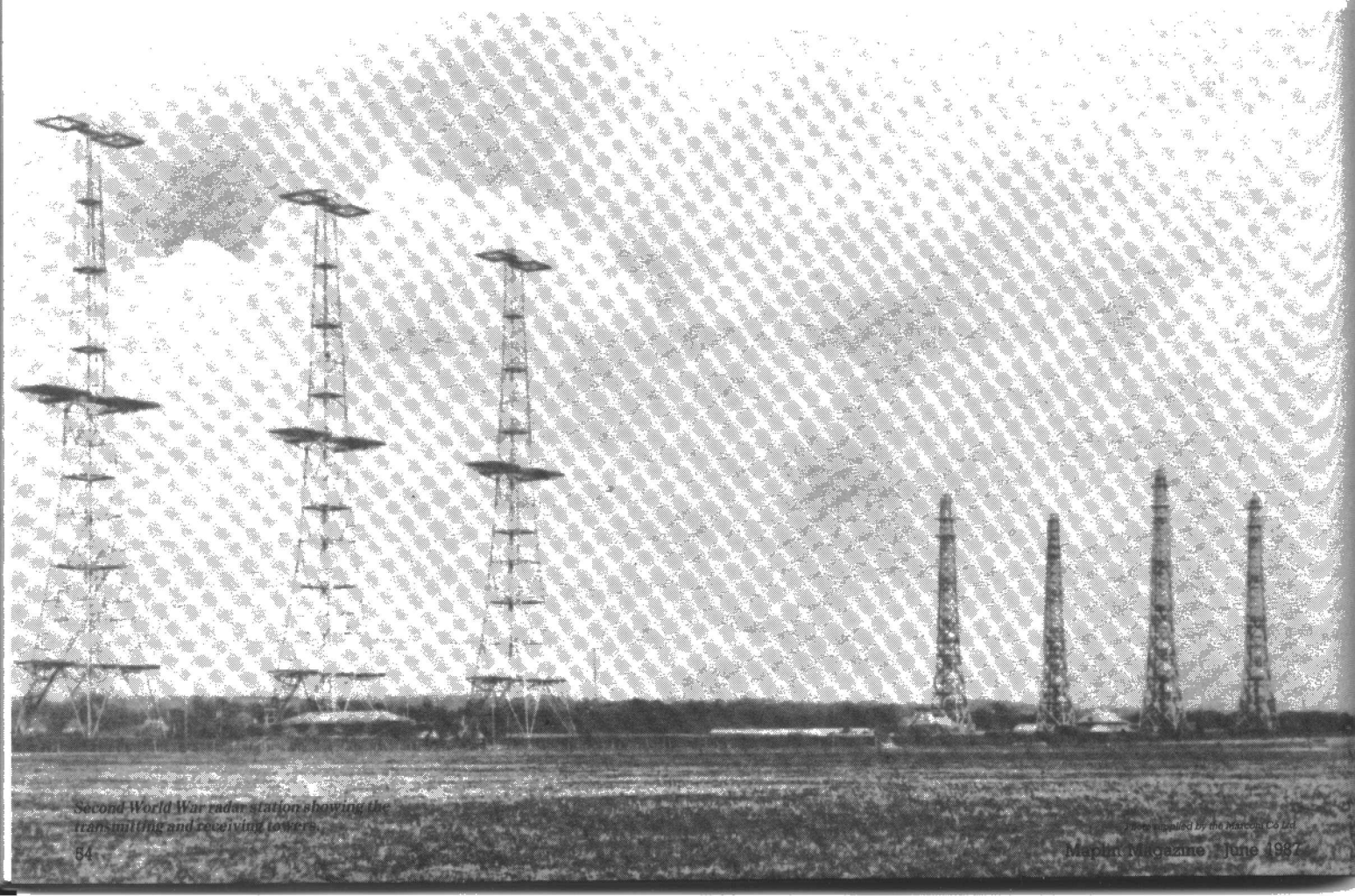
Part Seven– The Second World War

With the coming of the Second World War, the science of radio assumed enormous importance. One aspect of it, that played a vital role in the defence of this country in 1940, was 'radar'. This was an acronym apparently derived from the phrase, RAdio Detection And Ranging, though there are slight variations on this theme.

Early Radar

The need for radar arose from the necessity of being able to put fighters in the right place at the right time, in order to be able to intercept the streams of enemy bombers. Because of the time taken to reach operational altitude, sufficient advance warning of the enemies approach was vital. Standing patrols were not feasible because of the limited endurance of a fighter (e.g., maximum flying time for a Spitfire would have been only some fifteen minutes) and also because of the need to rest air crews between sorties. Some research into early warning systems had been done as far back as 1934, but based on acoustic techniques, using giant, 200 feet wide concrete 'mirrors' along our coastline, acting as parabolic sound collectors. However, in the few years available, radar (at first called R.D.F. for Radio Direction Finding) developed to the point where, in the Battle of Britain, it was possible to detect enemy aeroplanes at distances of 50 - 100 miles from our shores, and even to see the bombers circling their airfields in Normandy as they formed up for a raid.

Returning to 1934, it was in that year that the Committee for Scientific Survey of Air Defence was formed. Wimperis of this



Second World War radar station showing the transmitting and receiving towers.

Photo supplied by the Marconi Co Ltd.

committee wrote to R.A. Watson-Watt, of the Radio Department, National Physical Laboratory, Teddington, about the so-called 'death ray'. The outcome of getting Watson-Watt interested in the project was most significant.

This 'death ray' was a weapon beloved of fiction writers of the time and there were any number of unauthenticated claims for 'black boxes' that could kill rabbits at short range. The Air Ministry offered the sum of £1000 to any inventor who could demonstrate the killing of a sheep at 100 yards range with one of these devices. Needless to say, the sheep population of the British Isles was not one bit reduced by this offer!

However, what this piece of nonsense did achieve was to focus attention on the idea of energy concentrated in a ray of some form and, although this would not melt the aeroplane or even incapacitate any of its crew, Watson-Watt thought that by such a means it ought to be possible to locate the plan position of an aeroplane by measuring its distance from two reference points. The secret of this technique lies in timing a wave of known velocity. In the Imperial units of the day, this velocity was expressed as 186,000 miles per second, for radio waves. Energy reflected back from the aeroplane (a radio echo) gives a measure of the distance it is from the transmitter. For example, if the time between the transmitted wave and its received echo is measured as one millisecond, then the total distance travelled by the radio wave is given by:

Distance travelled = velocity x time
$= 1.86 \times 10^5 \times 1 \times 10^{-3}$
= 186 miles

Therefore, the object reflecting the radio wave lies at half this distance from the transmitter, namely 93 miles. An obvious way of displaying the result would be on the face of a cathode ray tube which, since it had hitherto been under development for television, was available at that time (see Story of Radio, Part Six). The type of display that would be presented is shown in Figure 1. The large 'pip' at the origin indicates the time of the transmitted pulse and the weaker pip to the right is the echo received from the target. Since there is a direct relationship between time and distance, the X scan can be calibrated directly in miles. Furthermore, the speed of the timebase can be switched to give different ranges. For example, it might initially be set at 200 miles to give an initial warning of enemy aeroplanes and then switched to 20 miles to give more accurate range as they drew closer. This principle was not entirely new as it had been used earlier to locate thunderstorms by detecting the presence of electrically charged clouds.

Initial tests on aeroplanes were carried out in the beam of the 50m Daventry transmitter, these simply proving that sufficient energy could be reflected from an aeroplane in flight for it to be possible to make measurements of range. From this small seed, sown in the spring of 1935, radar grew. Much of the credit for this pioneering work goes to Robert Watson-Watt, who was later knighted in recognition of the fact.

A team, under the leadership of the above, was set up and a suitable site found at Orfordness, on the Suffolk coast. Here the terrain was flat, ideal for the job. Tests began at the end of May 1935 and progress was rapid. Within six weeks, the equipment was detecting aeroplanes at ranges of 17 miles and, by July, the range had been increased to 40 miles.

Radar Improves

The more specific aims of the radar being developed were to give:

(a) plan position of hostile aeroplanes to an accuracy of within one or two miles, sufficient to be able to guide in a fighter in daylight in good visibility. There were two possible ways of doing this. In the first, two stations were used, the range from each being computed and the hostile being then located at the intersection of their arcs. In the second method, one station provided both range and bearing. These methods are illustrated in Figure 2.

(b) The approximate height of the enemy. This was obviously vital as it was no good sending in fighters to the right spot only to find when they got there that the enemy were 10,000 feet above or below them!

(c) The approximate size of the formations, since this dictated how many fighters to send in.

(d) Whether the aeroplane detected was friend or foe. This would be particularly important at night.

The identification of friend or foe was to elude the team for some time but, of the others, by the end of September 1935, a height of 7000 feet ± 1000 feet had been measured, and the problem of range measurement had been overcome.

It was now a question of putting theory into practice. An experimental system was constructed, using a low power transmitter and 70 feet masts. What was needed was very much higher power and taller masts. What was also needed was a whole 'chain' of such stations along the entire coastline facing Europe, together with some organisation to gather and distribute the information obtained to Fighter Command so that they could make the best use of it. A problem that was anticipated even at this stage was the likelihood that the enemy would attempt to 'jam' the radar with transmissions of their own. To avoid total loss of the radar facility under these conditions, there had to be several switched frequencies. The estimated cost ran into millions of pounds, even in the 1930's. However, the money was forthcoming because of the vision of those involved.

This nucleus of the Royal Radar Establishment (as it was later known) needed a new home and one was found at the mouth of the River Deben, Bawdsey Manor, still in Suffolk. This desirable site was bought from the owner by the Air Ministry. The new station opened in May 1936 and it continued in this role until September 1939, by which time a chain of radar stations stretched from Ventnor on the Isle of Wight to the Firth of Tay. The first operational radar station was the one at Bawdsey, and this was handed over to the Royal Air Force in May 1937. In August of that year, radar played its first active part in an R.A.F. defence exercise but this tended to reveal its weaknesses rather than its advantages, not the least being a certain ambiguity in the results obtained from different radar stations.

Credit should also be given to the firms that made the equipment of our first radar defence system. The transmitters were the work of Metropolitan-Vickers, the receivers were made by messrs. A.C. Cossor Ltd, while the Marconi Company made the transmitter antenna 'curtain' arrays.

Preparing for War

In September 1938 came the Munich crisis; from then on, through the inclement weather of the following winter, work went on to meet the war that was inevitable. From Good Friday of 1939, well before the actual start of World War Two (3rd September 1939), Britain's radar stations went on a 24-hour watch.

Radar stations were not only built to defend the British Isles. In those days, Britain exercised much influence abroad and needed radar to watch over strategic points overseas. The island of Malta is a good example where radar was later to play a vital part in the island's defence against the unceasing attacks of the German Luftwaffe and the Italian Regia Aeronautica.

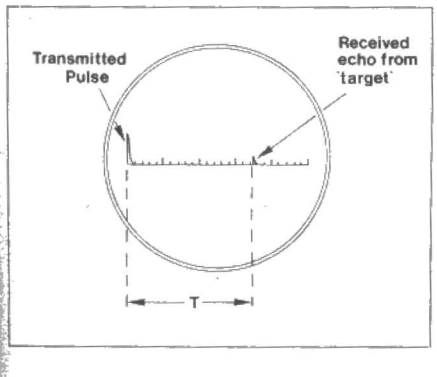


Figure 1. The basic principle of RADAR; the time T, the return journey time of the radio wave, is a direct measure of the distance to the target.

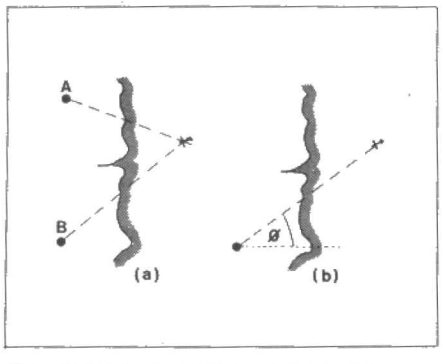


Figure 2. (a) The 'hostile' is located at the intersection of the beams from two stations, A and B. (b) A single station fixes both the range and bearing of the 'hostile'.

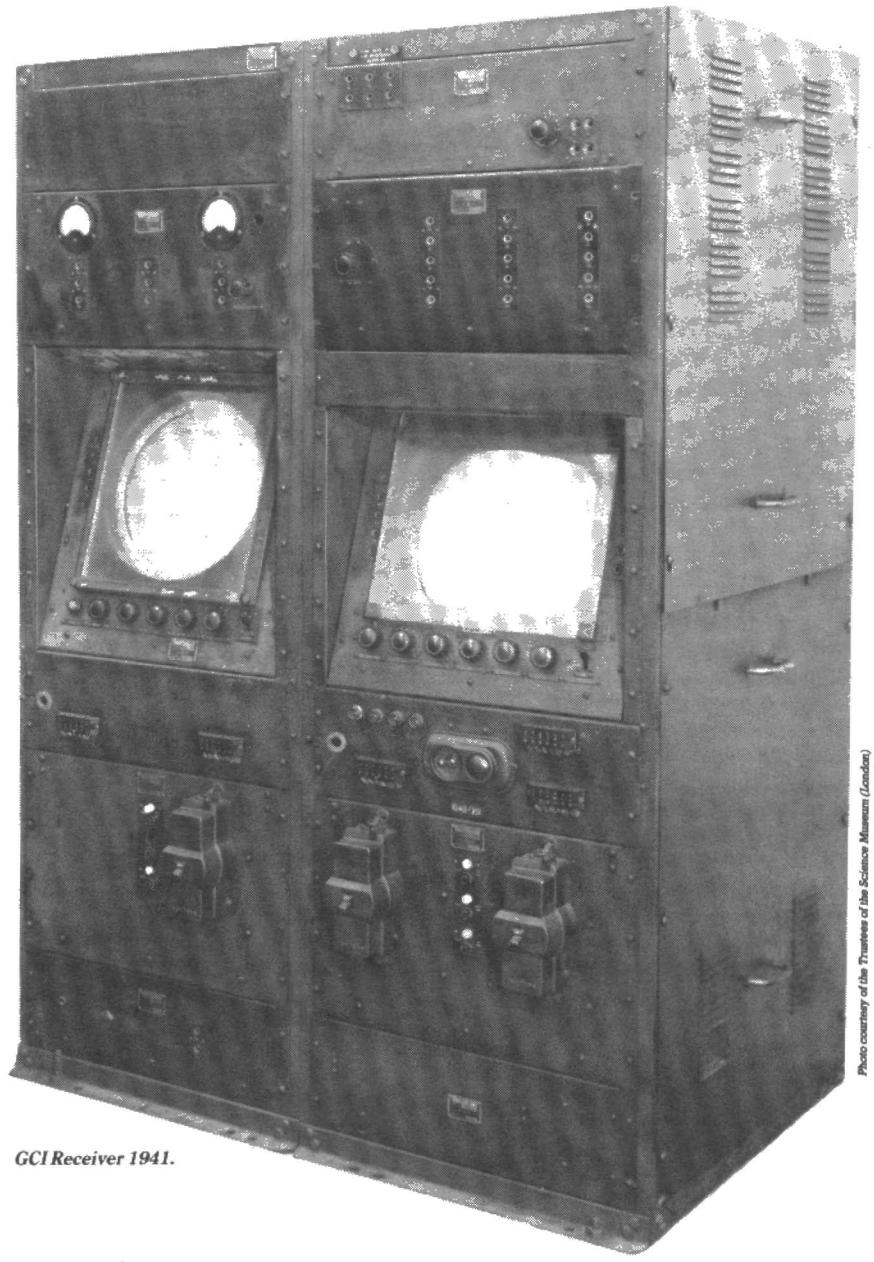
The early radar system that gave warning of impending air raids was known as Chain Home (C.H.). This radiated an enormous amount of power in attempting to 'floodlight' the area to the east of our coastline. It would obviously have been a more efficient use of power if it could have been concentrated into a beam, and the beam swung about to find the enemy aeroplanes. However, this was impossible because of the enormous size of the masts. Those for the transmitter were 350 feet high, and those for the receiver topped 240 feet! It is the difference between trying to find an object in a darkened room by either switching on the room lights, or standing at the door and swinging a torch about to locate it. The power of the torch bulb is a lot less than that of the room lighting.

The answer to this problem lay, of course, in the choice of wavelengths. As stated earlier, the initial tests used 50m, but this was reduced, first to 26m and then to 13m, giving improved results in detection. The C.H. stations used shorter wavelengths still, but they were still of the order of several metres. A further problem that arose with the long wavelengths and the design of the masts was the 'gap' that existed under the radar curtain. It was possible for a wave-skipping aeroplane to reach the coast undetected until the very last minute. Dover, and other coastal towns, received a number of unexpected visits in this way. It was obviously necessary to concentrate development on reducing the wavelength further while maintaining high power for good range. This development led to a power of 1kW coupled with a wavelength of 10cm, and to the birth of the 'magnetron', a special valve that was capable of generation at these high frequencies (a wavelength of 10cm corresponds to a frequency of 3GHz). This was in July of 1940. Later still it would be possible to generate hundreds of kilowatts at the same high frequencies. To use these short wavelengths effectively, the length of the pulse transmitted had to be very short. Whereas Chain Home used pulse lengths of the order of 10-25 microseconds, the pulse lengths on the centimetric waves were more like 0.25 microseconds in length.

Airborne Radar

The accuracies mentioned earlier were fine for daylight but not good enough for night interceptions where the defending aeroplane had to be almost on top of the intruder before there was any chance of a visual sighting. Obviously effort now had to be put into developing airborne radar. With this it would be possible for the defending pilot to be informed of the intruder's presence and probable location by radio and then use his own radar to get close enough to see it. Radars of this type were called A.I. for Airborne Interception.

The new A.I. radar in the air was allied with a new type of ground radar called G.C.I. for Ground Controlled Interception. This latter used a type of display called P.P.I. (Plan Position Indicator). P.P.I. showed a radius of about 50 miles, centred on a circular cathode ray tube. The 'pips' representing both the 'target' (enemy aeroplane) and the interceptor were shown on this display, their relative range and bearing being particularly easy to determine especially as the face of the display was marked out in grid squares. A display of this type is shown in Figure 3. The instructions from the ground controller were aimed at bringing the two pips mentioned into near alignment, at which point the defending pilot should be able to pick up the intruder on his own 'scope'. The fighter also carried a 'black box', known as I.F.F. (Identification Friend or Foe - the problem had at last been solved), which caused the 'friendly' pip to give a characteristic signal every few seconds.



GCI Receiver 1941.

Photo courtesy of the Trustees of the Science Museum (London)

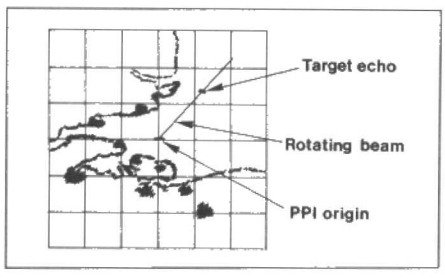


Figure 3. Typical return from PPI display. The rotating beam illuminates both the target and the main topographical features, e.g. coastline and towns. In this case the PPI equipment is on a ship in the Thames estuary.

The basis of P.P.I. was a rotating aerial system, giving a rotating beam. This type of scanner can now be seen at any airport, used with the airfield radar. The sweep time of the beam was about 20 seconds. A rotating line, like the spoke of a wheel, represented the radar beam. This was at quite low brilliance. However, when it picked up a reflection, perhaps from an enemy aeroplane, it glowed momentarily in a small arc. The persistence of the phosphors used was very much longer than that used with CRO's or television, in order to hold the image long enough for it to be picked up again on the next sweep. This was virtually the standard type of radar display during the war.

Electronic Warfare

As is now ancient history, radar played a vital part in the Battle of Britain. However, many other fascinating aspects of the story of radar could be told. One of these is the 'electronic warfare' that followed. The following gives a brief idea of what this involved.

Germany, in her attempt to find targets in Britain, was using a modified form of her

Lorenz beam system, known as 'Knickebein' (crooked leg). To counter this, we used jamming, which was at first generated using modified diathermy apparatus produced by Marconi and other companies, this being originally a sophisticated form of heat treatment equipment used in medicine. Later, powerful jamming transmitters were used. To combat these quite successful countermeasures, the Germans developed a new type of radar called 'X-Gerat'. This led in turn to more intensive jamming by the British. At the third level of development, the Germans produced 'Wotan', which was so effective that it had us scratching our heads for a time. But along came a solution in the form of 'beam-bending', by which the guidance beam apparently changed direction, causing the bomber to wander off on a wrong course. As a result, the poor old Luftwaffe expended their valuable armaments on the open countryside or even tried to make holes in the sea! And so it went on, each side gaining a temporary advantage.

Wartime Radio

As for 'radio' itself, perhaps one of the most famous pieces of equipment to be produced during the war was the development of a Marconi project begun in 1937. This was an airborne MF/HF transmitter-receiver known originally as the AD67/77. This subsequently became the T1154/R1155, of which more than 80,000 were made during World War Two. They were fitted in all aeroplanes of Bomber and Coastal Commands and were still in service in the 1950's.

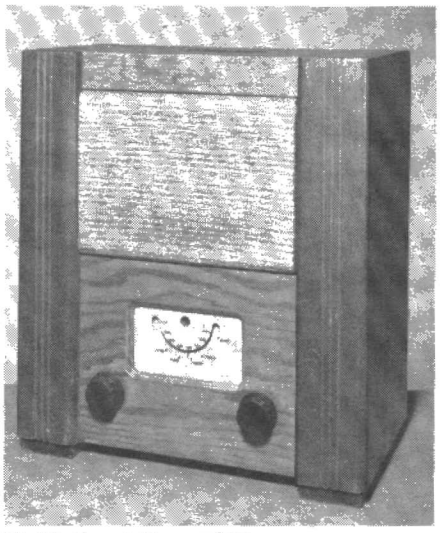


Photo courtesy of the Trustees of the Science Museum (London)

The Wartime civilian receiver.

At the outbreak of war all experimental licences were withdrawn. The role of the receiver was seen as a means of informing the public on the news and Civil Defence matters and providing entertainment to help boost morale. Programmes were often relayed in factories where many of the nation's women worked. A popular programme that began at this time and continued long after the war was 'Music While You Work'. On 1st September 1939, the Home Service, operating on a single nationwide frequency, replaced all National and Regional Programmes, this avoiding the possibility that the Regional transmitters might act as 'beacons' for enemy aeroplanes.

By November 1939 the BBC was transmitting two services for overseas listeners, the European Service and the World Service. At home, there was a great demand for receivers, especially portables. Shortage of spares, especially valves, brought the crystal set back into use, as a stand-by set at least. Home constructions became popular, particularly when the new 'battery valves', with their 1.4V heaters appeared. On 7th January 1940, the Forces Programme was introduced in order to cheer up the British Expeditionary Force in France.

On the 'home front' the demands of war meant that little effort could be spared for producing radio receivers to amuse the poor old civilians. Nonetheless, the British radio industry jointly produced a 'War-time Civilian Receiver' or 'Utility Set'. This was not, however, until July 1944 when the spares situation for existing sets, as well as the lack of trained personnel to service them, had made some form of replacement necessary. It was a fairly basic looking set and had only two stations marked on its dials, Home and Forces. It was to be a long time before effort was once again available for the pleasures of peace.

MACHINE CODE PROGRAMMING WITH THE Z80 *Continued from page 45.*

Interrupt Priority

It is usual to make the CTC a higher priority device than the PIO in the Z80 daisy-chain. The IEI input on the CTC is pulled up to logic 1 and the CTC's IEO output is then connected to the PIO's IEI input.

An Application Program

To show one possible way of using the CTC and illustrate some of the points made about programming it, Listing 2 gives a fully assembled and commented program that performs the following:

(a) Interrupts are enabled.
(b) Timer mode is selected.
(c) Pre-scaler is set to 256.
(d) Triggering is automatic.
(e) Time constant is set to &FF (255).
(f) Operation continues.

At the end of the timed interval, an interrupt will be generated that will call an Interrupt Service Routine. Because this could literally do anything it is not included though, for purposes of illustration, its vector is assumed to be &5DE0.

Finally, it is obviously useful to be able to compute the length of the timed interval. This is found from the product:

System clock period x pre-scaler value x time constant.

For example, for a 1MHz clock, a pre-scaler value of 256 and the maximum time constant of 256, the interval is 1.10^{-6} x 256 x 256, which equals 65.536ms.

The next part of this series will be the final one and will be concerned with a general look at writing machine code for the Z80.

```
00002  5000  (5000)          ORG   &5000
00003  5000  (00A0)  CCRO    EQU   &A0          ;&A0 is address of CCRO
00004  5000  FB              EI                ;Enable Z80 interrupts
00005  5001  ED 5E           IM    2           ;Set up Mode 2 interrupts
00006  5003  3E 5D           LD    A,&5D       ;HB of interrupt vector
00007  5005  ED 47           LD    I,A         ;Send it to I register
00008  5007  3E A5           LD    A,&A5       ;Control word
00009  5009  D3 A0           OUT   (CCRO),A    ;Send to CCRO
00010  500B  3E FF           LD    A,&FF       ;Time constant
00011  500D  D3 A0           OUT   (CCRO),A    ;Send to CCRO
00012  500F  3E E0           LD    A,&E0       ;LB of interrupt vector
00013  5011  D3 A0           OUT   (CCRO),A    ;Send to CCRO.
00014  5013  18 FE  LOOP     JR    LOOP        ;Wait for interrupt
00015  5DE0  (5DE0)          ORG   &5DE0       ;Interrupt vector
00016  5D00  (5D00)          ORG   &5D00       ;Interrupt Service Routine
00017  5D00  00      INTVEC  NOP               ;Dummy routine
00018  5D01  FB              EI
00019  5D02  ED 4D           RETI
```

Listing 2.

More MINI-CIRCUITS

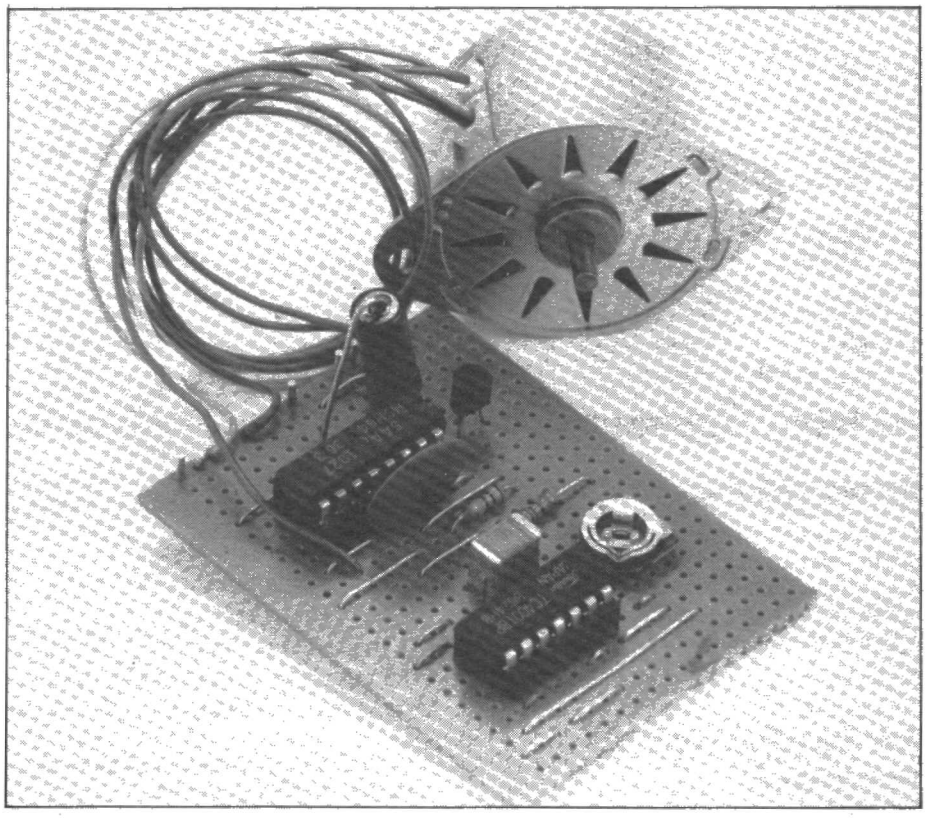
From Robert Penfold

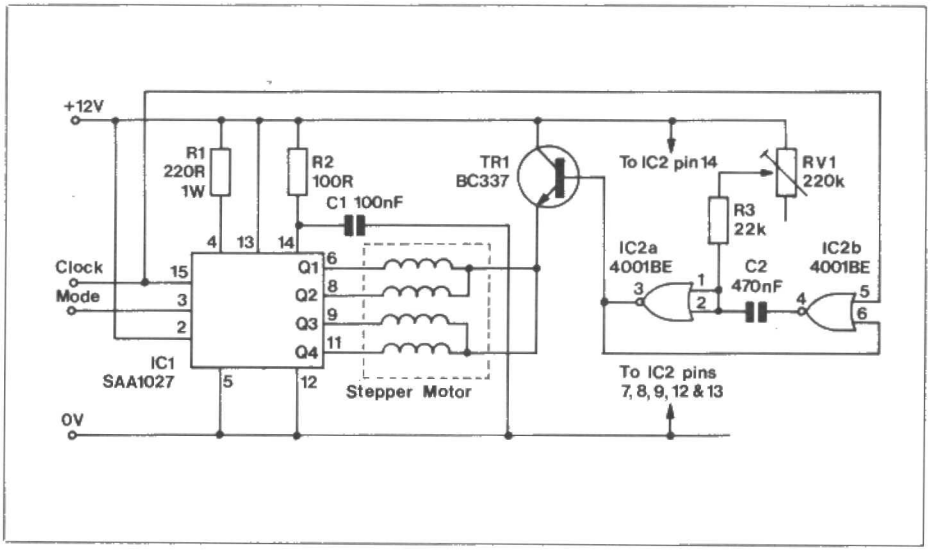
Stepper Motor Driver

The Mullard SAA1027 seems to have become the standard stepper motor driver device for home constructor designs, and it certainly offers good performance at relatively low cost. It is a fairly basic driver though, and it has the shortcoming of continuously driving the stepper motor with power even when it is not being stepped from one position to the next (for the uninitiated, with stepper motors it is the switching of power between its coils and not simply the application of power that operates the device). The continuous application of power is not likely to cause any damage to either the motor or the driver circuit, but it will often result in the motor running quite warm, and in an application where battery power is used it represents a terrific waste of the battery's capacity.

It is not difficult to incorporate some form of power economy circuit, and there are several possible approaches to the problem. The one used in the circuit shown here probably represents the best method as it does not require the use of any additional control lines from the computer or other controlling circuit, and it is totally 'invisible' to the user. It nevertheless cuts down the current consumption of the circuit to something very close to the minimum that can be achieved.

IC1 is the stepper motor driver, and this is really just the standard SAA1027 configuration. Pulses applied to the 'CLOCK' input step the motor, and the logic level applied to the 'MODE' input controls the direction of rotation. Although pin 2 is shown as connecting to positive supply rail, this can be used as a reset input if required, and it sets the outputs to their reset states (Q1 and Q3 low, Q2 and Q4 high) when it is taken to the low state. Note that the input signals must be between 7.5V and V+ for a 'high', and 0V to 4.5V for a 'low'. A simple level shifting circuit is therefore needed for control by ordinary 5 volt logic levels.





Stepper Motor Driver Circuit.

The current economy is obtained by having the 'common' terminals of the motor normally left open circuit, and only briefly connecting them to the positive supply rail when a clock pulse is received and IC1's outputs change state. This is achieved by having IC2 operate as a simple monostable multivibrator which is triggered by the clock pulses. Its output pulses activate TR1 which connects power through to the 'common' terminals of the motor. RV1 controls the monostable's output pulse duration, and this should be set for the minimum value which gives reliable operation of the circuit. Apart from minimising current consumption, this ensures that the monostable can provide output pulses at a rate which can match the stepping speed of the clock signal and the motor. The optimum pulse duration depends on the particular motor used, but the adjustment range of RV1 is sufficient to accommodate any normal type.

The reduction in static current consumption is likely to be quite large, but it is obviously dependent on the coil resistance of the motor concerned (which should have a resistance of about 75Ω or more through each coil). On test with a Maplin stepper motor (type No. 1) the prototype had a quiescent current consumption of just over 50 milliamps, which compares with about five to six times this figure without the power economy circuit. Of course, the amount of power saved in use depends on how often or otherwise the motor is stepped, but the saving will normally be quite substantial.

Only two gates of IC2 are utilised in this circuit, and the only connections to the other two are to tie their inputs to ground to protect them against static charges. Note that in the monostable configuration the 4011BE is not a suitable substitute for the 4001BE.

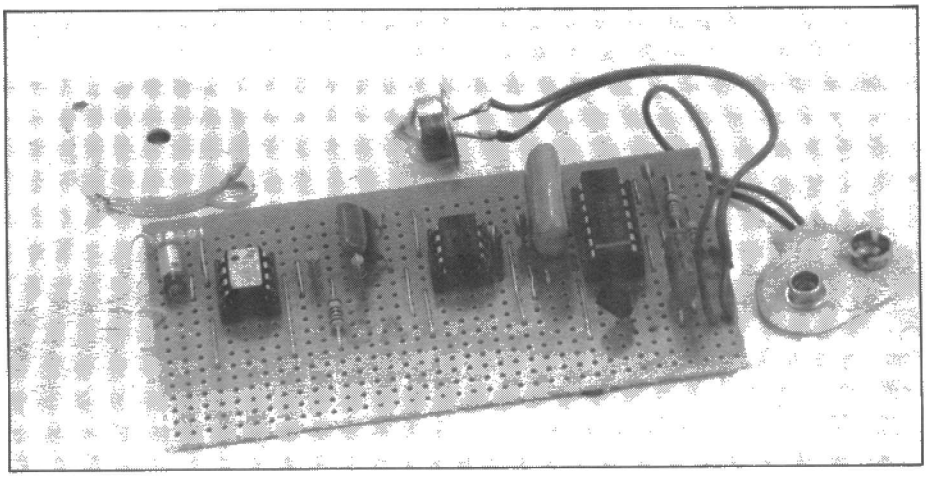
STEPPER MOTOR DRIVER PARTS LIST

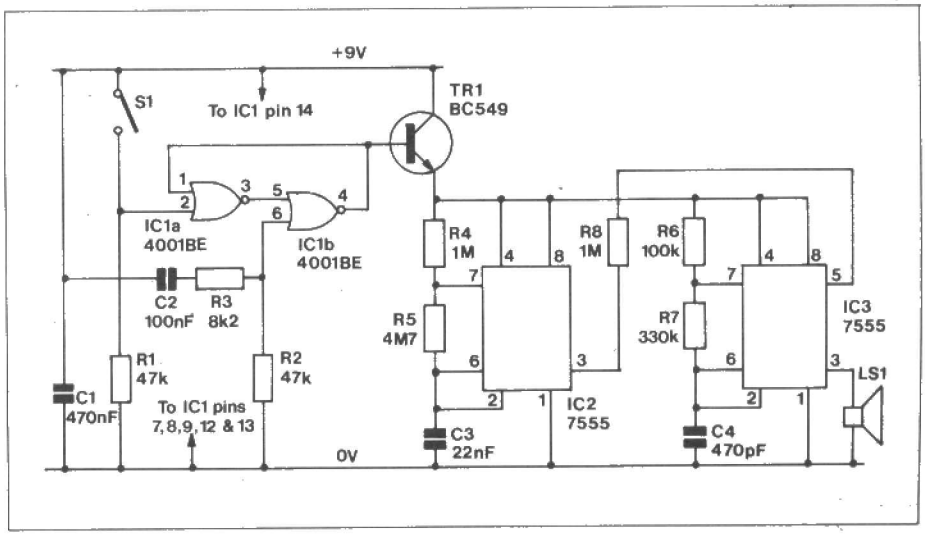
RESISTORS: All 0.6W 1% Metal Film unless specified			
R1	220Ω 1W	1	(C220R)
R2	100Ω	1	(M100R)
R3	22k	1	(M22K)
RV1	220k Hor Sub-min Preset	1	(WR62S)
CAPACITORS			
C1	100nF Ceramic	1	(YR75S)
C2	470nF Poly Layer	1	(WW49D)
SEMICONDUCTORS			
IC1	SAA1027	1	(QY76H)
IC2	4001BE	1	(QX01B)
TR1	BC337	1	(QB68Y)
MISCELLANEOUS			
M1	Stepper Motor Size 1	1	(FT73Q)
	DIL Socket 14-pin	1	(BL18U)
	DIL Socket 16-pin	1	(BL19V)

Movement Alarm

This simple but versatile alarm is triggered by movement of the unit, and it can be used in a variety of ways. As a burglar alarm it could be mounted on a door so that the unit is triggered when someone opens the door, and this could be the door of a car or caravan and not necessarily that of a building. The self-contained and portable nature of the unit also makes it well suited to applications such as a suitcase or television alarm, where the alarm will be activated if someone tries to remove the protected object. The unit could be made quite compact, making it suitable as protection for practically anything valuable which cannot be reliably screwed down.

There are various types of sensor which could be used, but a mercury switch is the obvious type to opt for. This type of switch is basically just two electrodes in a container made of an insulating material, and partially filled with mercury, where at some orientations the mercury only comes into contact with one or neither of the electrodes so that there is a very high resistance between them, but at other orientations the mercury touches both electrodes and completes electrical contact between the two. In an application of this type the switch should be set so that it is just off a point where it provides electrical contact, so that any slight movement or vibration at least momentarily activates the switch and triggers the alarm circuit.





Movement Alarm Circuit.

Basically, all that the circuit has to do is to provide a latching action from what might only be a momentary switching action from the sensor, and then use this signal to drive some form of audible alarm generator. If the unit is to be battery powered, it must also have an extremely low stand-by current consumption so that it can be left operating for long periods of time without significantly discharging the battery. In this design the latching is provided by a conventional set/reset flip/flop formed by IC1a and IC1b. The other two NOR gates of IC1 are left unused, but their inputs are tied to the negative supply rail in order to protect them against static charges, and also to ensure that the unused gates have an insignificant current consumption. In fact, by using a CMOS latch the quiescent current consumption of the circuit is kept down to just a fraction of a microamp, and it was found to be immeasurably low with my test gear. C2 provides the initial 'reset' pulse, to set the flip/flop to the correct output state at switch-on, while S1 is the mercury switch which sets the output to the high state when it is activated.

The output of the latch controls the alarm generator circuit via emitter follower buffer stage TR1. The latter is a silicon device with a low leakage level so that when the alarm is switched off it does not consume a significant amount of current. The alarm generator circuit is based on two 555 astable circuits with IC3 providing the audio tone and IC2 frequency modulating it. The modulation is obtained by loosely coupling the output of IC2 to the control voltage input of IC3 via R8, and this gives a simple but effective two tone 'warbling' alarm sound. LS1 is a cased ceramic resonator which gives high efficiency and a penetrating output at the relatively high audio frequencies involved here. If optimum volume is important, R7 can be replaced by a 1M preset which can then be adjusted to find the two frequencies which provide the greatest output.

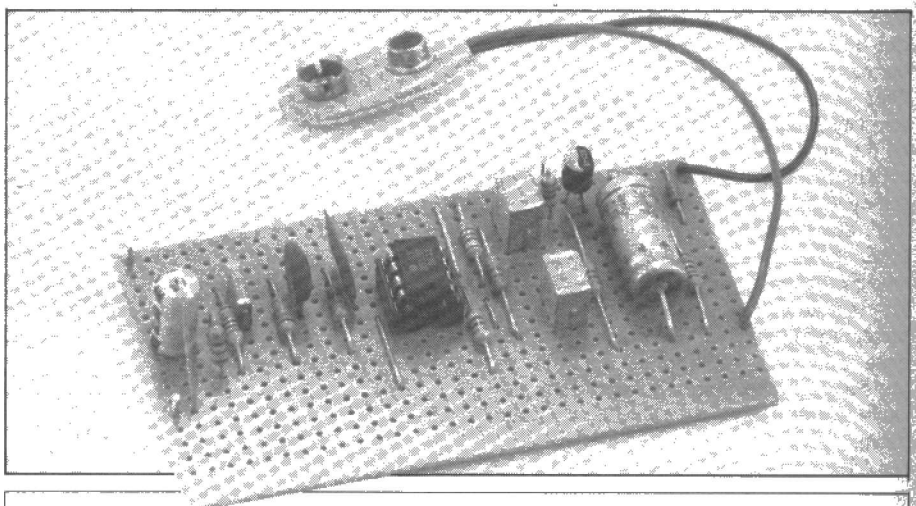
MOVEMENT ALARM PARTS LIST

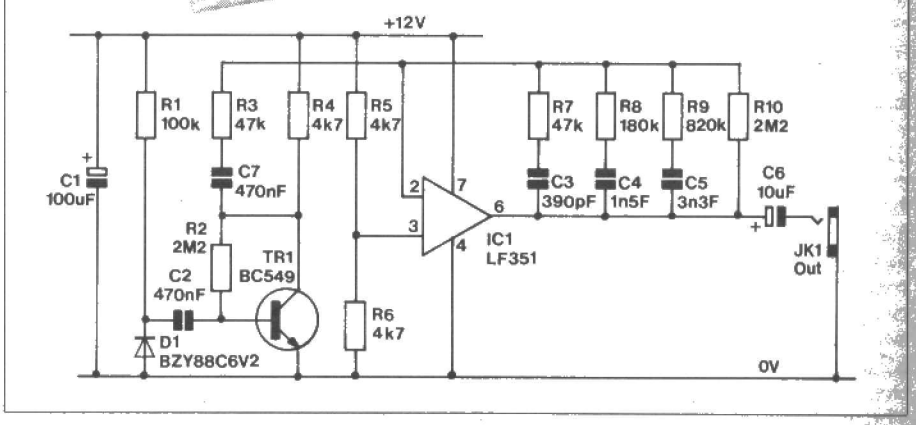
RESISTORS: All 0.6W 1% Metal Film			
R1,2	47k	2	(M47K)
R3	8k2	1	(M8K2)
R4,8	1MΩ	2	(M1M)
R5	4M7Ω	1	(M4M7)
R6	100k	1	(M100K)
R7	330k	1	(M330K)
CAPACITORS			
C1	470nF Poly Layer	1	(WW49D)
C2	100nF Poly Layer	1	(WW41U)
C3	22nF Poly Layer	1	(WW33L)
C4	470pF Polystyrene	1	(BX32K)
SEMICONDUCTORS			
IC1	4001BE	1	(QX01B)
IC2,3	ICM7555	2	(YH63T)
TR1	BC549	1	(QQ15R)
MISCELLANEOUS			
S1	Mercury Switch	1	(FA76H)
LS1	Piezo Sounder	1	(FM59P)
	DIL Socket 8-pin	2	(BL17T)
	DIL Socket 14-pin	1	(BL18U)

Pink Noise Generator

'White noise' is a well known term in the electronics world, and it is generally thought of as the 'hissing' background sound produced by audio circuits. White noise has a more precise definition though, and it is a noise signal which has equal amplitude at all frequencies. In other words, there is the same energy in (say) any 100Hz wide chunk of the spectrum, and would therefore be the same energy from 100Hz to 200Hz as there would from 20000Hz to 20100Hz. Logarithmic scaling is normally used on the frequency axis in frequency response charts, etc., and this is a more realistic way of looking at things. This has equal energy in octave or decade frequency bands, or to take a simple example, there would be the same amount of energy from 100Hz to 200Hz as there would from 20000Hz to 40000Hz.

The noise generated by audio circuits is generally of the genuine 'white' variety and is free from any significant colouration unless the circuit includes de-emphasis or some other form of frequency response tailoring. While white noise is ideal for many applications where noise is a help rather than a hinderance (percussion synthesisers, etc.), there are occasions when the alternative of 'pink' noise is required.





Pink Noise Generator Circuit.

This type of signal has equal energy over octave or decade bands, and could be regarded as noise having logarithmic scaling rather than the linear scaling of white noise. As far as the sound is concerned, white noise has the familiar high pitched 'hissing' sound, whereas pink noise is a deeper 'rushing' sound which is often likened to the sound of rain falling.

Pink noise is primarily used in audio testing, and in particular it is used in conjunction with an audio analyser as a very quick means of displaying irregularities in the frequency response of audio equipment. The main point here is that with the noise signal fed direct to the input of the analyser, all channels should indicate the same input level. Any lack of flatness in the frequency response, or anything interposed between the noise source and the analyser will be instantly and clearly displayed on the analyser.

It is probably impossible to directly generate pink noise, and it is therefore produced by first generating a white noise signal and then applying top cut filtering. This is the method adopted in the circuit shown here which uses zener diode D1 as the noise source, TR1 as a high gain amplifier to boost the noise signal to a usable level, and IC1 as an inverting amplifier with frequency selective negative feedback to provide the tailoring of the frequency response. The required slope is 3dB per octave, which is awkward in practice as a single stage C-R filter provides double this. Consequently a three stage feedback network is required, with a resistor added in series with each filter capacitor to prevent it from ever providing the full 6dB per octave roll-off. C3 provides the high frequency roll-off, with C4 and C5 providing the filtering at middle and bass frequencies respectively. The typical output level is around 2 volts peak to peak from a low source impedance, and the current consumption of the circuit is only about 4 milliamps. When constructing and using the unit, bear in mind that it has a substantial voltage, particularly at low frequencies, and it is therefore quite sensitive to pick-up of mains 'hum'.

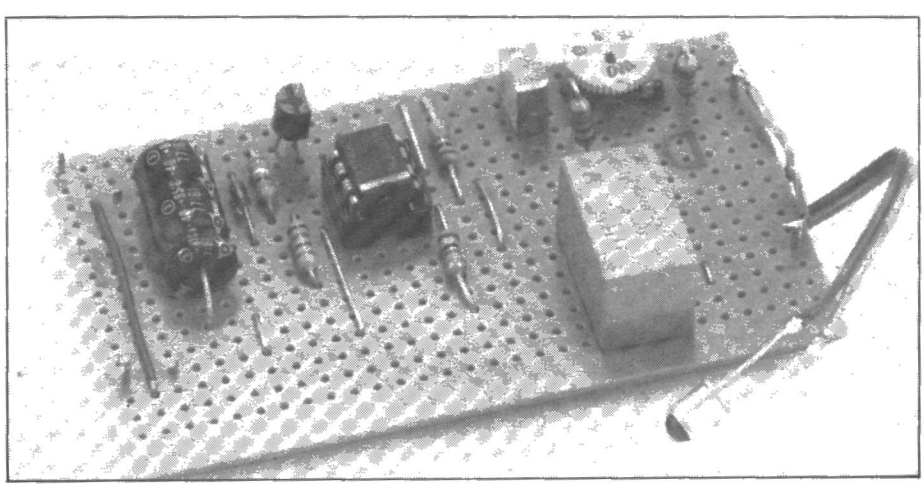
PINK NOISE GENERATOR PARTS LIST

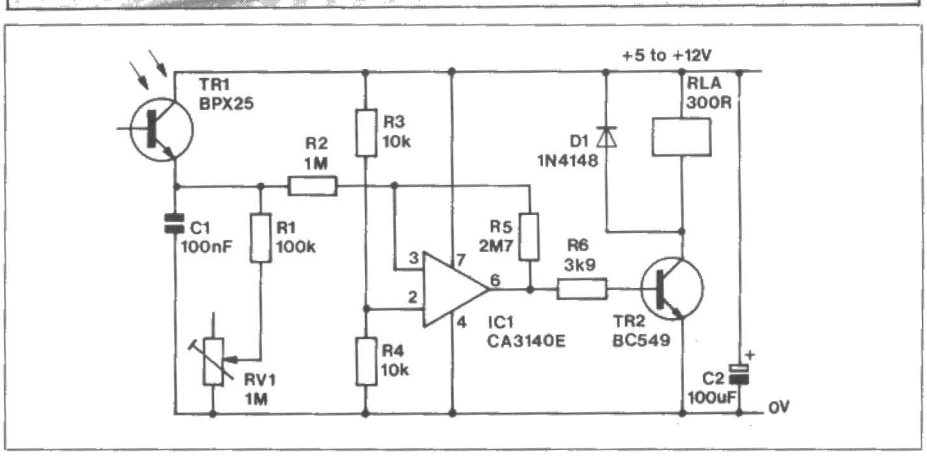
RESISTORS: All 0.6W 1% Metal Film			
R1	100k	1	(M100K)
R2,10	2M2Ω	2	(M2M2)
R3,7	47k	2	(M47K)
R4,5,6	4k7	3	(M4K7)
R8	180k	1	(M180K)
R9	820k	1	(M820K)
CAPACITORS			
C1	100μF 35V Axial Electrolytic	1	(FB49D)
C2,7	470nF Poly Layer	2	(WW49D)
C3	390pF Ceramic	1	(WX63T)
C4	1n5F Poly Layer	1	(WW23A)
C5	3n3F Poly Layer	1	(WW25C)
C6	10μF 50V PC Electrolytic	1	(FF04E)
SEMICONDUCTORS			
IC1	LF351	1	(WQ30H)
TR1	BC549	1	(QQ15R)
D1	BZY88C6V2	1	(QH09K)
MISCELLANEOUS			
JK1	3.5mm Jack Socket	1	(HF82D)
	DIL Socket 8-pin	1	(BL17T)

Opto-Port

The standard approach to controlling external devices from a computer is to either use a built-in port such as a user or printer port, or to add a few latches onto the expansion bus. If a number of output lines are required this is certainly the most practical method, and probably represents the only practical way of doing things. If, on the other hand, only one or two output lines are required and operating speed is not of prime importance there are simple alternatives. The main two are to use either the sound output or the screen to control a simple switching circuit, and the circuit shown here is a simple screen operated switch (which is more generally applicable than the sound activated type).

In principle this type of circuit is very straightforward, with a photocell aimed at a small area of the screen. A simple software routine lights up that area of the screen to switch on the controlled device, or blanks out that part of the screen in order to switch it off. Things are complicated very slightly by the fact that the scanning process which is used to build up the television or monitor display results in a strong 50Hz ripple on the output from the photocell, and the circuit must smooth this out in





Opto-Port Circuit.

order to give a clean output signal. It is this factor which gives very limited operating speed in comparison to a conventional computer output port, but performance is still adequate in this respect for the majority of applications, including the obvious one of a relay driver.

TR1 is the photocell, and the TIL81 phototransistor is a fair choice for this as it offers good directivity, reasonable sensitivity, and is cheap (but more expensive devices such as the BPX25, which is the device shown in the circuit and Parts List, and the BPY62 will work in the circuit just as well, as will virtually any silicon npn phototransistor). It is used here as a sort of light dependant resistor with no connection being made to its base terminal. When subjected to darkness only minute leakage currents flow through TR1, giving virtually zero volts at its emitter terminal. When subjected to a reasonably strong light source quite high leakage currents flow, resulting in the voltage at its emitter approaching the positive supply voltage.

This gives roughly the required switching action, but the noise infested and high impedance output of TR1 needs to be both cleaned up and buffered in order to give a useful output signal. C1 smooths out much of the noise on the output signal, but its value has been kept low enough to keep the switching time down to a fraction of a second. This leaves a significant amount of noise on the signal, but this is counteracted by the large amount of hysteresis in the trigger circuit based on IC1.

OPTO-PORT PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1	100k	1	(M100K)
R2	1MΩ	1	(M1M)
R3,4	10k	2	(M10K)
R5	2M7Ω	1	(M2M7)
R6	3k9	1	(M3K9)
RV1	1MΩ Hor Sub-min Preset	1	(WR64U)
CAPACITORS			
C1	100nF Poly Layer	1	(WW41U)
C2	100μF 35V Axial Electrolytic	1	(FB49D)
SEMICONDUCTORS			
IC1	CA3140E	1	(QH29G)
TR1	BPX25	1	(QF30H)
TR2	BC549	1	(QQ15R)
D1	1N4148	1	(QL80B)
MISCELLANEOUS			
RLA	Ultra-min Relay 12V DPDT	1	(YX95D)
	DIL Socket 8-pin	1	(BL17T)

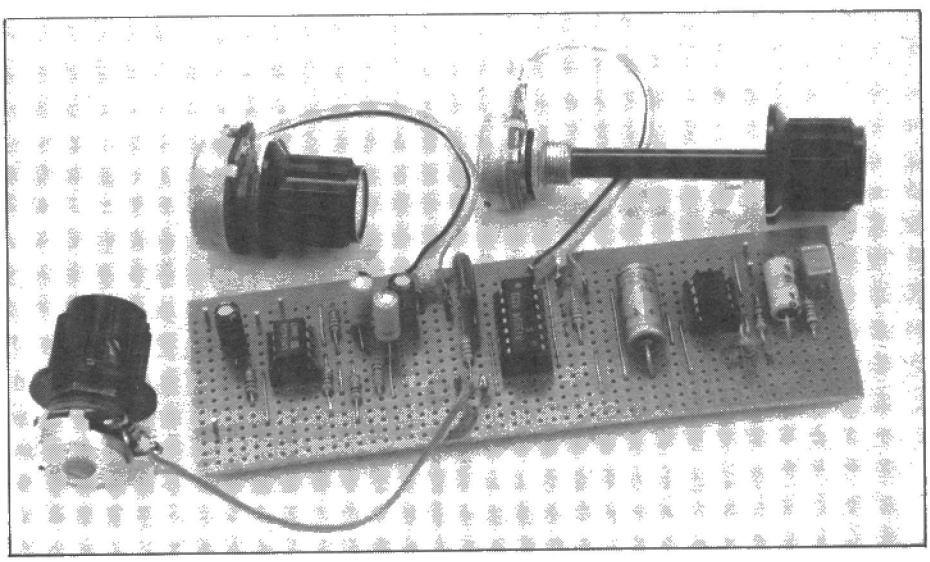
TR2 operates as the relay driver, and the relay can be any type with a coil resistance of around 300Ω or more, and a suitable operating voltage. The supply voltage can be anything from 5 to 12 volts, and must be chosen to suit the particular relay used. If a TTL compatible output is required it is merely necessary to use a 5 volt supply, omit D1, and to replace the relay with a 1kΩ resistor. Note though, that switching on the on-screen character sends the output low and not to the high state.

The circuit is quite sensitive and TR1 does not have to be fitted right up against the screen, although it will probably need to be no more than about 30 millimetres away. It is not necessary for the on-screen character to be a solid block, and something like a '@' symbol should suffice. TR1 is quite directional and must therefore be aimed at the character quite accurately. RV1 is adjusted by trial and error to find a setting that gives reliable results, and the exact setting will be very critical.

Metal Pedal

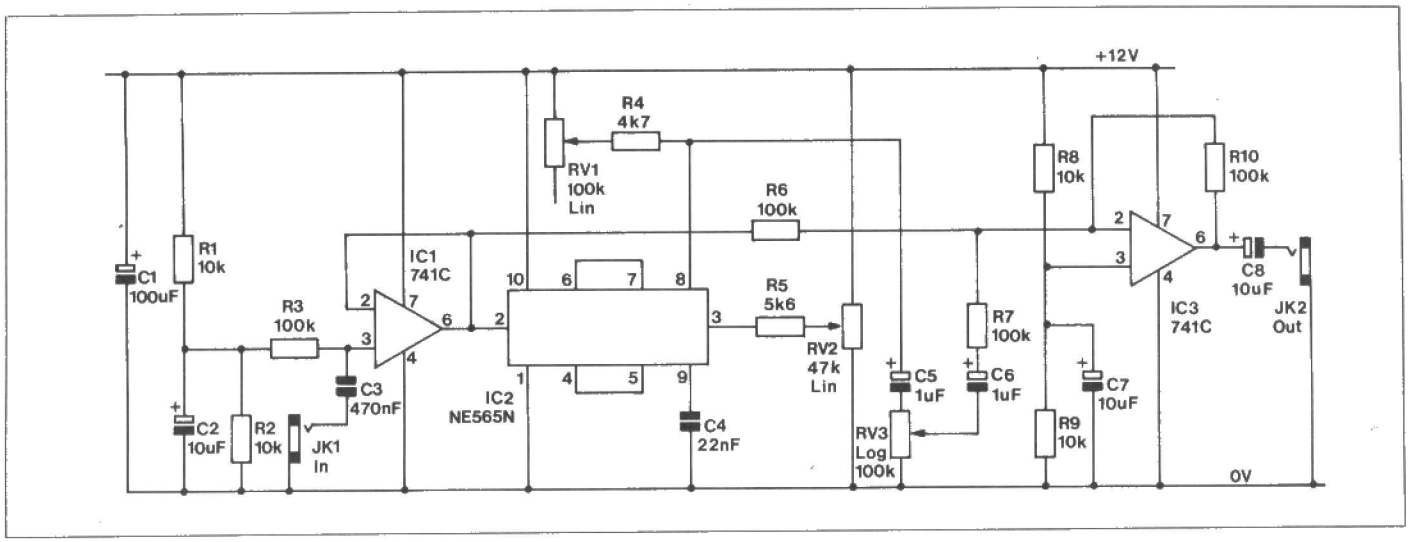
While not perhaps to everyone's taste, the so-called 'metal' sound is now an established electronic musical effect. Technically it is produced by mixing two signals creating sum and difference frequencies, neither of which are normally harmonically related to the original input frequencies. The result can be very discordant, or with the two input frequencies spaced at suitable musical intervals the result is a very rich sound, like bells, gongs, and similar metalic instruments (hence the 'metal' name).

The effect is simple in theory, but in practice it can be more difficult to get really good results. The usual set-up is to have a variable frequency oscillator feeding one input of the mixer (or 'ring modulator' as it is generally known in this application), with the output from a guitar or other instrument feeding into the second input. The ring modulated signal is then mixed into the straight-through signal in the required quantity. The usual problem is that of breakthrough of the oscillator signal at the output, and even if the ring modulator gives a respectable 40dB or so of carrier suppression this still leaves a clearly audible signal under no



input conditions. A noise gate is therefore normally required in order to render the breakthrough inaudible.

In this design, the need for a noise gate is avoided by having a very high degree of carrier suppression in the ring modulator, and the latter is actually the phase comparator of an NE565N phase locked loop (IC2). The VCO stage of this device acts as the carrier oscillator, and it provides a frequency range of approximately 100Hz to 2kHz with RV1 acting as the frequency control. RV2 is the carrier balance control, and this is carefully adjusted to minimise the carrier breakthrough at the output. It is a front



Metal Pedal Circuit.

panel control rather than a preset, as the optimum setting varies very slightly with changes in the carrier frequency, and although a good compromise setting can be found it was felt to be better to have the ability to null out the carrier as much as possible. The maximum degree of carrier suppression seems to be quite high, with around 80dB being achievable with the prototype.

IC1 simply acts as an input buffer stage which provides the unit with an input impedance of about 100kΩ. Its output is direct coupled to the input of IC2, for which it provides with the necessary input bias voltage. IC3 acts as a conventional summing mode mixer circuit which combines the modulated and straight-through signals. RV3 controls the amount or ring modulated signal that is mixed into the unprocessed signal. Signal levels of up to about 8 volts peak to peak can be handled using a 12 volt supply (the use of a 9 volt battery supply is not recommended). The current consumption is about 10 milliamps.

METAL PEDAL PARTS LIST

RESISTORS: All 0.6W 1% Metal Film			
R1,2,8,9	10k	4	(M10K)
R3,6,7,10	100k	4	(M100K)
R4	4k7	1	(M4K7)
R5	5k6	1	(M5K6)
RV1	100k LIN Pot	1	(FW05F)
RV2	47k LIN Pot	1	(FW04E)
RV3	100k LOG Pot	1	(FW28C)
CAPACITORS			
C1	100μF 35V Axial Electrolytic	1	(FB49D)
C2,7,8	10μF 50V PC Electrolytic	3	(FF04E)
C3	470nF Poly Layer	1	(WW49D)
C4	22nF Poly Layer	1	(WW33L)
C5,6	1μF 100V PC Electrolytic	2	(FF01B)
SEMICONDUCTORS			
IC1,3	μA741C (8-pin DIL)	2	(QL22Y)
IC2	NE565	1	(WQ56L)
MISCELLANEOUS			
JK1,2	Standard Jack Socket	2	(HF91Y)
	DIL Socket 8-pin	2	(BL17T)
	DIL Socket 14-pin	1	(BL18U)

AMENDMENTS TO 1987 CATALOGUE

BLUE SEAL BATTERY R03B (Page 42). This is no longer available. FK54J is now being supplied as Silver Seal R03S.

SLOPING FRONT CASE XY60R (Page 78). Please note that this case does not have ventilation holes as described in the 1987 catalogue.

0.1in. PC EDGCONN 2 X 20-WAY (Page 129). In the order code list, this should be stock code BK97F and not BK87F.

VIDEO COPYING KIT RK71N (Page 136). The second lead in the audio list should be 5-pin DIN socket to 2 phono plugs.

SOLID ALUMINIUM KNOBS K8A YR64U (Page 176). The fixing nut on the pots sold by Maplin will not fit inside the recess provided in the knobs. This also applies to knob K10A (RK89W).

PLASTIC LENS FA95D (Page 201). This lens is not 'clear' but coloured red.

STYLUS CLEANER FLUID FV38R (Page 283). This is now supplied in a larger, new style bottle with an integral brush, but no instructions.

4K7 ENCLOSED PRESET UH15R (Page 293). In the description following the stock code for this item in the catalogue this is referred to as being horizontal mounting, whereas it is in fact vertical mounting.

ZTX750 to ZTX753 (Page 300). In the semiconductor list, these devices (UH50E to UH53H) are shown as NPN transistors, they are in fact PNP types.

74HC4511 (Page 327), cannot drive common anode LED's directly. It will drive common cathode LED's directly via a series resistor (same as the 4511BE). However for driving common anode LED's inverter/buffers are needed.

74HC4351 8-WAY ANALOGUE SWITCH UF14Q (Page 329). This is a 20 pin device, and not 18 pin.

LM1037 (Page 346). There are some changes to the diagram of the Dual 4-channel analogue switch (QY33L). Externally pin 5 is connected to C1 and +Vs. However, in the internal schematic representation of the IC, pin 5 should not connect to anything.

ICL7673 BATTERY BACKUP IC UH36P (Page 370). In the diagram for the high current system for the ICL7673, please note that the input is not 'Mains Supply' but should be 'Main supply' - *do not connect 240V AC to this chip.*

ICL7660 VOLTAGE CONVERTER YY75S (Page 370). Last line of description should read 'a supply voltage of +5V the output voltage will be −4.3V.' (not 15V).

MAX232C (Page 379). The 22μF capacitor which is shown connected between pin 2 and earth should instead be shown to connect to +5V (pin 16) with the capacitor positive to pin 2.

SQUARE 3½in. MYLAR SPEAKER (Page 395). YN02C has an impedance of 4Ω, and not 8Ω.

FOOT SWITCH FH92A (Page 410). The description of the terminals and their operation for this switch are no longer correct. The description should be: SPDT switch. The common terminal is the centre of three solder tags. Rated 2A at 250V AC Body size: 36 x 12 x 15mm. Bush and knob length: 28mm.

AUDIO OSCILLATOR MA204 YM66W (Page 429). Third sentence states external frequencies can be connected. Although prototypes had this feature, production models will not. Frequency counter will function from internal source only. Stock of this item & YM68Y, Function Generator MG205, will not be with us until mid-May 1987.

15V MINIATURE TRANSFORMERS WB15R & LY03D (Page 457). Please note that the descriptions of these two items heve been transposed. WB15R is the 6VA version and LY03D is the 10VA type. This also applies to the physical dimensions given.

UHF MODULATORS UM1233, UM1286, FT30H & BK66W (Page 464). Types UM1233 and UM1286 have a wider and more linear bandwidth to cater for the chroma sub-carrier from a source video generator, they do not generate the chroma subcarriers internally. Same applies to the 6MHz sound carrier for the UM1286. The terminal designation letters A - D in the lower table apply to all units where the unit is turned label upwards and terminal wires are at left-hand side - UM1111 & UM1233 will have phono socket pointing away at top.

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SERVICE MANUAL or circuit diagram for Texas instrument data terminal type 743KSR, EIA/TTY (UK). Write to D.J. Looker, 202 Farmers Close, Witney, Oxon OX8 6NS.

PENSIONER WOULD LIKE TO BUY TV magazine June 1984, or photostat of component tester, signal generator 5.5 – 55MHz, wavemeter. Offers, collect. E.E. Matthews, 63 The Oval, Otley, West Yorkshire LS21 2EE.

WANTED ALL PCB's FOR SPECTRUM synthesiser, and/or full circuit diagrams, component suppliers, construction details for TV dishes, receivers, etc. Reply to: A. Trstenjak, 49 Deacon Ave., Kempston, Bedfordshire MK42 7DU.

WANTED CX1441 MODULES for Solartron CD1400 'scope; also CX1443 module. Write to Mr. Guppy, Flat 8, 27 Lansdown Place, Cheltenham, Gloucestershire GL50 2HX. Tel: 0242 575346 (evenings).

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LOAN OR BUY circuit diagrams and manual for Televet model 877. Also circuit diagram for 'Beamec' CRT tester made by Grünther. W.T. Moorby, 83 Kellet Road, Canforth, Lancashire LA5 9LR.

ANY INFORMATION on Mael 4000 computer. Write to Mr. J. House, Church View, Atherington, Umberleigh, Devon EX37 9HY. Tel: Barnstaple (0271) 79073 before 5.00 pm.

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CORRIGENDA

Vol. 6 No. 22

Test Gear & Measurements: Page 12; the second equation in the first column should read: '$N^2 = V^2 + I^2 - 2VI \cos \Theta$.'

Hi-Fi Loudspeakers and Enclosures: Page 21; at the bottom of the centre column the text should read: "squaring F_s, multiplying this by V_{as}, dividing the result by V_b etc."

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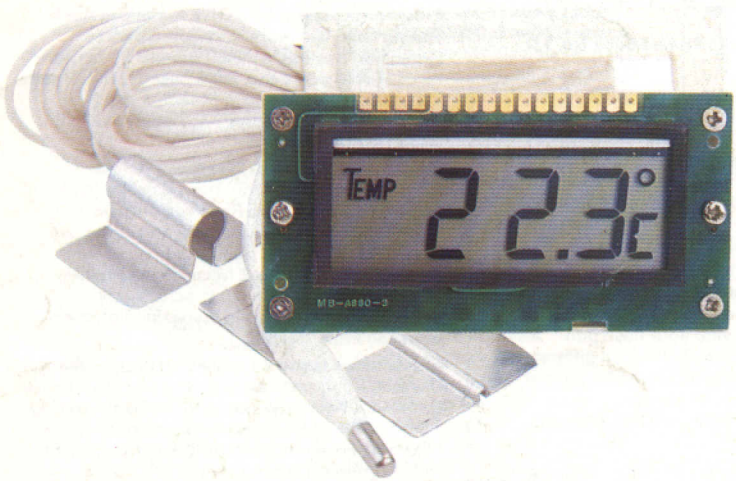

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